M8K1553MCH

MIL-STD-1553
Test and Simulation Module for the
EXC-8000 Family of Carrier Boards

User's Manual

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Table of Contents

Figures

Tables

1 Introduction

Chapter 1 provides an overview of the *M8K1553MCH* avionics communication board. The following topics are covered.

1.1 Overview

The *M8K1553MCH* is an intelligent, single function, double-sized, MIL-STD-1553 interface module for the multimode, multiprotocol Excalibur EXC-8000 family of carrier boards. The *M8K1553MCH* provides a complete solution for developing and testing 1553 interfaces and performing system simulation of the MIL-STD-1553 bus. All standard variations of the MIL-STD-1553 protocol are handled by the module.

The *M8K1553MCH* contains 32k × 16 of dual-port RAM for Data blocks, Control registers, and Look-up tables. All Data blocks and Control registers are memory-mapped and may be accessed in real time.

The dual-redundant 1553 module may be programmed to operate in one of four modes of operation: Bus Controller, Remote Terminal, RT/Concurrent-Bus Monitor, and Bus Monitor. The *M8K1553MCH* comes complete with Windows software, and a C driver software library including source code, and one mating connector.

The *M8K1553MCH*-E option is an extended temperature (-40° to +85°C), ruggedized version of the module for industrial or harsh environmental conditions.

Note Although this manual uses **byte** addressing, values in pointer registers use **word** addressing. For example, the Operational Status register is listed at address 0002 H, which is 2 bytes from the beginning of memory. (See **Operational Status Register** on page 3-5.) But if the value of the Interrupt Log List Pointer register is 3000, the Interrupt Log List starts 3000 words (or 6000 bytes) from the beginning of memory. (See **Interrupt Log List Pointer Register** on page 3-8.)

1.1.1 *M8K1553MCH* Module Features

General Features

- Single function, independent, dual-redundant double-sized module
- Ruggedized and extended temperature options available (-40° to +85°C)
- Operates as BC, RT, BM or RT/Concurrent-BM
- Supports MIL-STD-1553A/B
- Autonomous operation in all modes
- 32K x 16 dual-port RAM
- 32 Control registers
- Polling or interrupt driven
- Real-time operation
- Built-in Test capability
- Direct or Transformer bus coupling modes
- 16-bit 64 µsec Time Tag

Bus Controller Mode

- Advanced message control features
- Major/Minor frames
- Programmable intermessage gap
- Programmable automatic retry

Remote Terminal Mode

- Single RT simulation
- Double buffering of data
- Circular buffer mode
- Message illegalization
- Programmable broadcast mode

Bus Monitor Mode

- Filtering per RT
- Interrupt history list
- Programmable monitor block count

Physical Characteristics

- Dimensions: 46mm x 60.5mm
- Weight: 32g

Operating Environment

- Operating Temperature: 0° to +70°C standard
  -40° to +85°C extended temp. (optional)
- Storage Temperature: -55° to +125°C standard
- Humidity: 5% to 90% noncondensing
- MTBF: 426,730 hours at 25°C, GF, S217F

Host Interface

- EXC-8000 family of carrier boards
- Power: 5V @ 260mA (0% duty cycle)
  5V @ 860mA (87% duty cycle)

Software Support

- *1553MCH Software Tools*: Intuitive and flexible API with source code
  - Compatible with 32/64-bit Windows 7/8/10/11 & Linux kernel 3.x/4.x/5.x
  - Includes application interface for NI LabView & CVI
- *Merlin MCH Bus Analyzer* for Windows

See **Chapter 8: Ordering Information** for exact part numbers.

1.1.2 *M8K1553MCH* Block Diagram

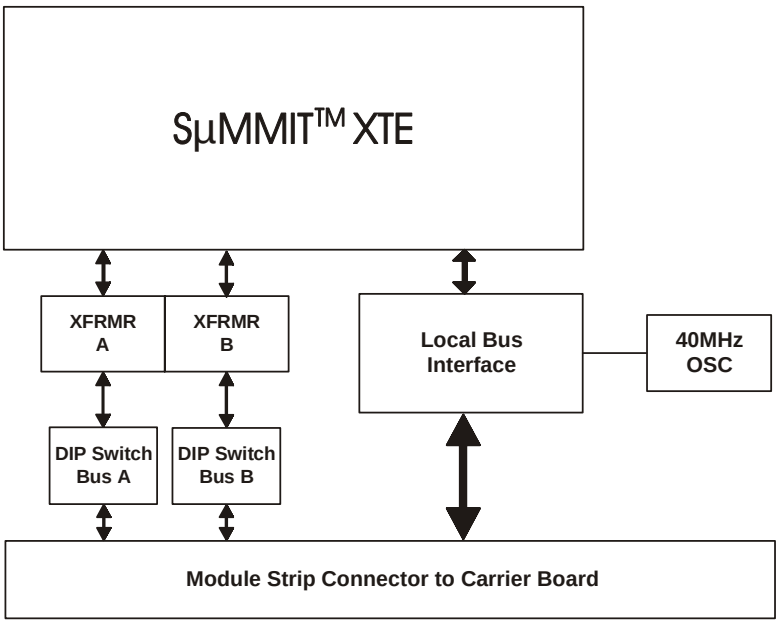

Figure 1-1 *M8K1553MCH* Block Diagram

1.2 Installation

For hardware and software installation instructions, see **`Installation Instructions.pdf`** in the root folder of the installation CD. When downloading new software from the Excalibur website, **`Installation Instructions.pdf`** is contained in the zip file.

The *Excalibur Installation CD* you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. For more details, see **`Installation Instructions.pdf`**. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.2.1 Module Installation

Warning Make sure that you are grounded for electrostatic discharge when handling the Excalibur device, and use all antistatic precautionary measures.

1553 devices may be connected to the 1553 bus either directly (direct-coupled) or via a bus-coupling stub (transformer couple. See Figures 1-2 and 1-3. Use DIP switches SW1 and SW2 to set the coupling mode to the 1553 bus(es). See section **7.3 Module Coupling Mode DIP Switches [SW1–SW2]** on page 7-3.

1.3 1553 Bus Connections

For short distances, direct coupling may be used to connect the *M8K1553MCH* directly to another 1553 device. To ensure data integrity, you must make certain that the cable connecting the two devices is properly terminated with 78-Ohm resistors (see Figure 1-2).

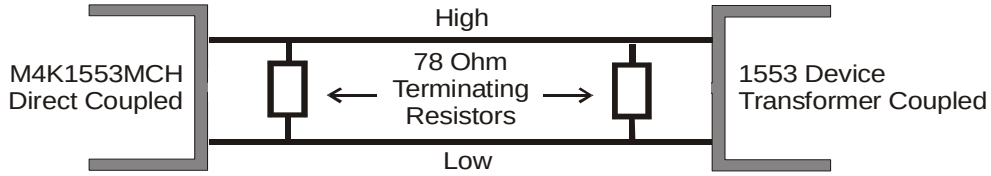

Figure 1-2 Direct coupled connection (one bus shown)

If operating in the more standard Transformer coupling mode, use stub coupler devices, which are available from Excalibur Systems. Two terminators are required for each coupler, which services a single bus, i.e. BUS A (see Figure 1-3). For more information see our website: www.mil-1553.com.

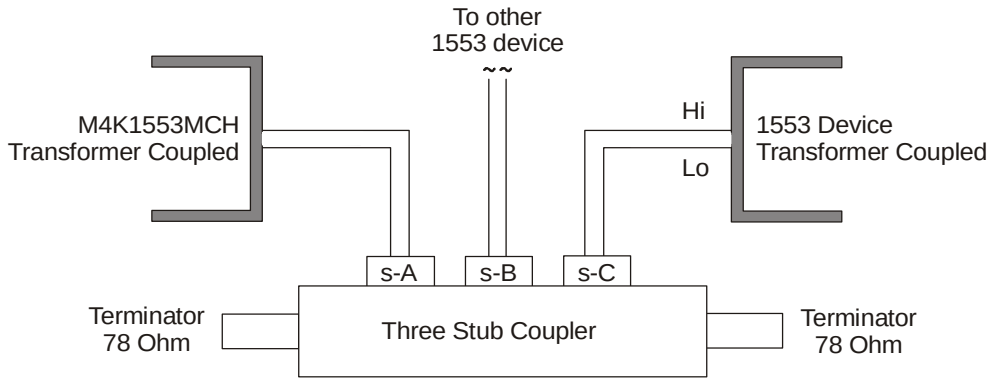

Figure 1-3 Transformer coupled Connection (one bus shown)

Example of MIL-STD-1553 Bus Connection

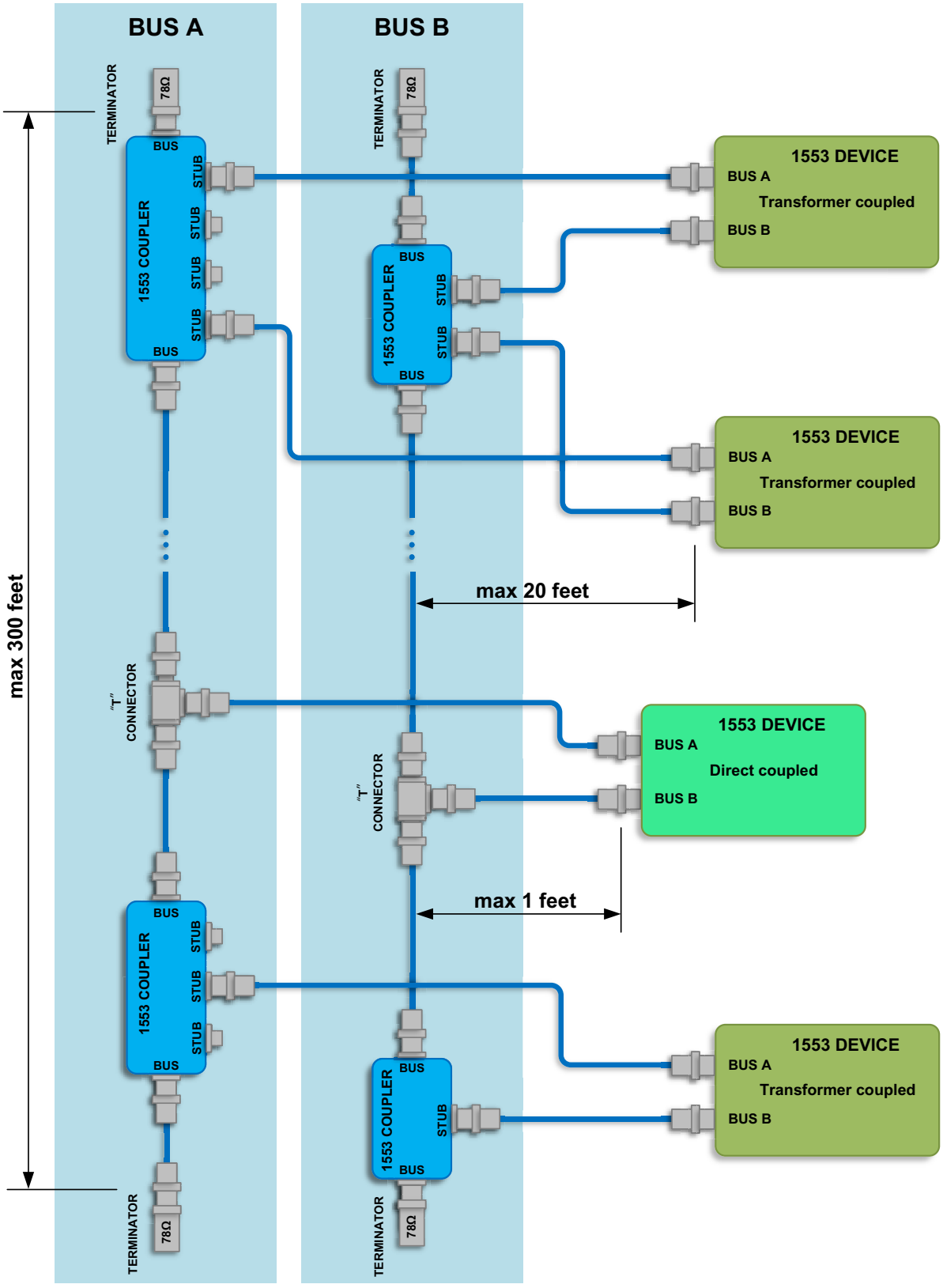

Figure 1-4 MIL-STD-1553 Bus Connection

1.4 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, visit the Technical Support page of our website (www.mil-1553.com). You can also contact us by phone. To find the location nearest you, visit to the Contact Us page of our website. Before contacting Technical Support, please see Information Required for Technical Support.

2 Memory Address Space

Chapter 2 describes the *M8K1553MCH*'s Memory Address Space.

The *M8K1553MCH* occupies a 32K-word area of the module's Memory Address Space. This area is shared between the:

- Module Register Block, for the 32 control registers
- Module Memory Block, for data and message control
- External Timer Clock Register, to set the external timer clock value and the
- Module Reset Register to carry out the software reset of the module.

A powerful RISC processing unit (UTMC "SμMMIT™-XTE" 1553 protocol controller) provides automatic message handling, message status, general operational status and interrupt information. The user has direct access to all control registers and data blocks in Real Time. The *M8K1553MCH* may be configured to support MIL-STD-1553A as well as MIL-STD-1553B protocol.

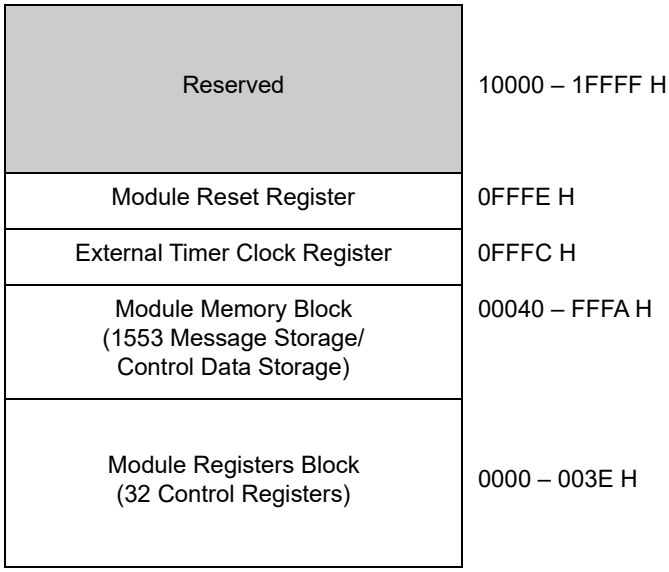

Figure 2-1 Module Memory Map

Chapters 3, 4 and 5 of the *User's Manual* explain the operation of the *M8K1553MCH* module in each of the three modes: Bus Controller, Remote Terminal, and Bus Monitor. In each chapter the mode specific Control Registers and Memory Block are described.

2.1 External Timer Clock Register

Address: BASE+0FFFC (H)
Read/Write

The External Timer Clock Register selects the external timer clock value for the module's timer. In normal operation, the module uses an internal fixed clock (64 µsec.). However, the module can be programmed to use an external, user-defined clock. (See the ETCE (bit 10) in Bus Controller **Control Register** on page 3-4 and Bus Monitor Mode **Control Register** on page 5-4.)

The clock is derived from the PCI base board's HTTCLK signal (1 MHz). There are two reasons to use the external clock:

A desired timer resolution different from the fixed one (64 µsec.)

A request for the timers synchronization to the PCI base board's clock and/or synchronization to other modules residing in the PCI base board.

A hardware or software reset will reset the external timer clock to its default value (64 µsec). The external timer clock has a range of 4 µsec (250 KHz) to 126 µsec (7.94 KHz)

Bit	Description
06-15	Don't care
00-05	Timer Clock Value **Valid values:** 0001 (H) (250 KHz) – 003E (H) (7.94 KHz)

External Timer Clock Register

To formulate the Timer Clock Value (TCV):

$$TCV = \frac{1,000,000}{2 \times F} - 1$$

F = Desired frequency (HZ) — 7.94 KHZ–250 KHz

Example: Desired programmable Timer Clock frequency is 10 KHz (100 µsec) resolution:

$$TCV = \frac{1,000,000}{2 \times 10,000} - 1 = (50 - 1) = 49\text{Dec} = 31(\text{H})$$

Write 00031 H to the register.

2.2 Module Reset Register

Address: BASE+FFFE (H)
Write

Writing to the Module Reset Register (data = don't care) performs a software reset of that module. The module will act as if the power had been switched off and then on.

Note Writing to this register immediately terminates command processing. The reset operation takes 5µsec to execute.

3 Bus Controller Operation

Chapter 3 describes *M8K1553MCH* operation in Bus Controller (BC) mode. The topics covered are:

3.1 Bus Controller Message Processing

To process messages, the *M8K1553MCH* uses data supplied in the control registers along with data stored in RAM memory. The module accesses eight words stored in RAM memory called a command block. The command block is accessed at the beginning and end of command processing.

Note In BC mode, the module does not need to re-read the Command Block on a retry situation.

The user allocates memory spaces for the minor frame. The top of the command blocks can reside at any address location. Defined and entered into memory by the user, the control registers are linked to the Command Block via the Command Block Pointer Register contents. Each command block contains a:

Control Word
Command Word1
Command Word2
Data Pointer
Status Word 1
Status Word 2
Branch Address
Timer Value

Figure 3-1 Command Block Architecture: BC Mode

See section **3.3 BC Architecture** on page 3-10 for a description of each location.

Control Word information allows the module to control the commands transmitted over the 1553 bus. The Control word allows the module to transmit commands on a specific bus, perform retries, initiate RT-to-RT transfers, and interrupt on certain conditions. The host defines each Command Word associated with each command block. For normal 1553 commands, only the first Command Word location will contain valid data. For RT-to-RT commands, as specified in the Control Word, the host must define the first Command Word as a receive and the second Command Word as a transmit.

For a receive command, the Data Pointer is read to determine where Data Words are retrieved. The module retrieves Data Words sequentially from the address specified by the Data Pointer. For a transmit command, the Data Pointer is read to determine the top memory location. The module stores Data Words sequentially from this top memory location.

The module reads the command block during minor frame processing. The module then begins the acquisition of Data Words for either transmission or storage.

After transmission or reception, the module begins post-processing. The command block is updated. The module modifies the Control Word as required. An optional interrupt log entry is performed after the command block update.

3.2 Control Registers: BC Mode

The control registers are read/write unless otherwise stated. All control registers must be accessed in word mode. All control register bits are active high and are reset to 0 unless otherwise stated.

Figure 3-2 below illustrates the control registers for Bus Controller mode.

Reserved	0012 - 003E H
Command Block Pointer Register	0010 H
Minor Frame Timer	000E H
BIT Word Register	000C H
Interrupt Log List Pointer Register	000A H
Pending Interrupt Register	0008 H
Interrupt Mask Register	0006 H
Current Command Block Register	0004 H
Operational Status Register	0002 H
Control Register	0000 H

Figure 3-2 Control Registers Map: BC Mode

3.2.1 Control Register

Address: 0000 (H)
Read/Write

Use the Control register to configure the module for BC mode operation. To make changes to the BC and this register, the STEX bit (Bit 15) must be logic 0

Bit	Bit Name	Description
15	**STEX**	Start Execution 1 = Initiates module operation 0 = Inhibits module operation After execution begins, writing a logic 0 will halt the module after completing the current 1553 message.
14	**SBIT**	Start BIT 1 = Places the module into the Built-In Test routine. The BIT test takes 1 msec. to execute and has a fault coverage of 93.4%. Once the module has been started, the host must halt the module in order to place it into the Built-In Test mode (STEX = 0). **Note** If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
11-13	**Reserved**	Set to 0
10	**ETCE**	External Timer Clock Enable 1 = Enables an external clock used with an internal counter for variable minor frame timing **Note** The user can only change the clock frequency before starting the device (i.e. setting bit 15 of register 0 to a login 1.
09	**ERTO**	Extended Response Time-Out 1 = Enables the extended response time-out option and forces the BC Mode to look for an RTs response time in 30 μsec. or generate time-out errors. 0 = Enables for the standard time-out in 14 μsec.
05-08	**Reserved**	Set to 0
04	**BCEN**	Broadcast Enable 1 = Enables the broadcast option for BC Mode. 0 = Enables Remote Terminal #31 as a unique remote terminal address. When enabled, the module does not expect a Status Word response from the Remote Terminal.
03	**Reserved**	Set to 0
02	**PPEN**	Ping-Pong Enable. This bit controls the method by which the module will retry messages. 1 = Allows the module to ping-pong between buses during retries. 0 = All retries will be performed on the programmed bus as defined in the Retry Number field of the Command Block control word.
01	**INTEN**	Interrupt Log List Enable. 1 = Enables the interrupt log list. 0 = Prevents the logging of interrupts as they occur.
00	**Reserved**	Set to 0

Control Register

3.2.2 Operational Status Register

Address: 0002 (H)
Read/Write

The Operational Status register provides pertinent status information for BC Mode and is not reset to 0000 H on reset. Instead, the bit A/B_STD is set to 1.

Note To make changes to the BC and this register, the STEX bit (Bit 15 in the Control Register) must be logic 0.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**MSEL1**	Mode Select 1. In conjunction with Mode Select 0, this bit determines the module's mode of operation.
08	**MSEL0**	Mode Select 0. In conjunction with Mode Select 1, this bit determines the module's mode of operation.

MSEL1	MSEL0	Mode of Operation
0	0	BC
0	1	RT
1	0	BM
1	1	RT/ Concurrent BM Mode

07	**A/B_STD**	Military Standard 1553A or 1553B. This bit determines if the module will operate under MIL-STD-1553A or 1553B protocol. 1 = Forces the module to look for all responses in 9 μsec. or generate time-out errors. 0 = Automatically allows the module to operate under the MIL-STD-1553B protocol (see section **3.6 MIL-STD-1553A/B Operation: BC Mode** on page 3-18
04-06	**Reserved**	These read-only bits are not applicable.
03	**EX**	Module Executing. This read-only bit indicates whether the module is presently executing or is idle. 1 = The module is executing. 0 = The module is idle.
02	**Reserved**	This read-only bit is not applicable.
01	**Ready**	Module-Ready. This read-only bit is cleared on reset. 1 = The module has completed initialization or BIT, and regular operation may begin.
00	**TERACT**	module Terminal Active. This read-only bit is cleared on reset. 1 = The module is presently processing a 1553 message. **Note** When STEX transitions from 1 to 0, EX and TERACT stay active until command processing is complete.

Operational Status Register

3.2.3 Current Command Register

Address: 0004 (H
Read only

The Current Command register contains the last 1553 command that was transmitted by the module. Upon the execution of each Command Block, this register will automatically be updated. This register is updated when transmission of the Command Word begins. In an RT-to-RT transfer, the register will reflect the latest Command Word as it is transmitted.

Bit	Bit Name	Description
00-15	**CC[15-0]**	Current Command. These bits contain the latest 1553 command that was transmitted by the Bus Controller.

Current Command Register

3.2.4 Interrupt Mask Register

Address: 0006 (H)
Read/Write

The BC Mode interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked only if the corresponding bit of this register is set to a logic 0.

Bit	Bit Name	Description
12-15	**Reserved**	Set to 0
11	**MERR**	Message Error Interrupt
06-10	**Reserved**	Set to 0
05	**EOL**	End Of List Interrupt
04	**ILLCMD**	Illegal Command Interrupt
03	**ILLOP**	Illogical Opcode Interrupt
02	**RTF**	Retry Fail Interrupt
01	**CBA**	Command Block Accessed Interrupt
00	**Reserved**	Set to 0

Interrupt Mask Register

3.2.5 Pending Interrupt Register

Address: 0008 (H)
Read only

The Pending Interrupt register is used to identify which of the interrupts occurred during operation. The assertion of any bit in this register generates an interrupt.

Note All register bits are cleared on a host read.

Bit	Bit Name	Description
12-15	**Reserved**	Ignore on read.
11	**MERR**	Message Error Interrupt 1 = A message error occurred. The module can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated (if not masked) after message processing is complete.
06-10	**Reserved**	Ignore on read.
05	**EOL**	End Of List Interrupt. 1 = The module is at the end of the command block.
04	**ILLCMD**	Illogical Command Interrupt. The module checks for RT-to-RT Terminal address field match, RT-to-RT transmit/ receive bit mismatch and correct order, and broadcast transmit commands. If illogical commands occur, the module will halt execution. 1 = An illogical command (i.e., Transmit Broadcast or improperly formatted RT-to-RT message) has been written into the Command Block.
03	**ILLOP**	Illogical Opcode Interrupt. 1 = An illogical opcode (i.e., any reserved opcode) was used in the command block. The module halts operation if this condition occurs.
02	**RTF**	Retry Fail Interrupt. 1 = All programmed retries failed.
01	**CBA**	Command Block Accessed Interrupt. 1 = A command block was accessed (Opcode 1010), if enabled.
00	**Reserved**	Ignore on read.

Pending Interrupt Register

3.2.6 Interrupt Log List Pointer Register

Address: 000A (H)
Read/Write

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts.

The *M8K1553MCH* architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K-word memory space. Initialize the lower 5 bits of this register to a logic 0 by the host. The module controls the lower 5 bits to implement the ring-buffer architecture. Read this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Bit	Bit Name	Description
00-15	**ILLP[15-0]**	Interrupt Log List Pointer Bits. **Note** Bits 05-15 indicate the starting Base address while bits 00-04 indicate the ring location of the Interrupt Log List.

Interrupt Log List Pointer Register

3.2.7 BIT Word Register

Address: 000C (H)
Read/Write

The BIT Word register contains information on the current status of the module hardware. The user defines the lower 8 bits of this register.

Bit	Bit Name	Description
15	**DMAF**	DMA Fail. 1 = All the module's internal DMA activity was not completed within 16 μsec.
14	**WRAPF**	Wrap Fail. The module automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is set. The loopback path is via the MIL-STD-1553 bus transceiver.
13	**Reserved**	Ignore on read
12	**BITF**	BIT Fail. 1 = A BIT failure. Interrogate bits 11 through 08 to determine the specific failure.
11	**BUAF**	Bus A Fail. 1 = A BIT test failure in Bus A.
10	**BUBF**	Bus B Fail. 1 = A BIT test failure in Bus B.
09	**MSBF**	Memory Test Fail. Most significant memory byte failure.
08	**LSBF**	Memory Test Fail. Least significant memory byte failure.
00-07	**UDB[7-0]**	User-Defined Bits.

BIT Word Register

3.2.8 Minor Frame Time Register

Address: 000E (H)
Read only

The Minor Frame Timer register (MFT) reflects the state of the 16-bit MFT counter. This counter is loaded via the Load Minor Frame Timer opcode (Opcode 1110).

Bit	Bit Name	Description
00-15	**MFT[15-0]**	Minor Frame Timer. These bits indicate the value of the timer.

Minor Frame Time Register

3.2.9 Command Block Pointer Register

Address: 0010 (H)
Read/Write

The Command Block Pointer register contains the location to start the Command Blocks. After execution begins, this register is automatically updated with the address of the next block.

Bit	Bit Name	Description
00-15	**CBA[15-0]**	Command Block Address. These bits indicate the starting location of the Command Block.

Command Block Pointer Register

3.3 BC Architecture

As defined in MIL-STD-1553, the Bus Controller initiates all communications on the bus. To comply with MIL-STD-1553 bus controller requirements, the *M8K1553MCH* uses a Command Block architecture that takes advantage of both control registers and RAM. Each Command Word transmitted over the bus must be associated with a Command Block. The Command Block requires eight contiguous 16-bit memory locations for each message.

These eight locations include a:

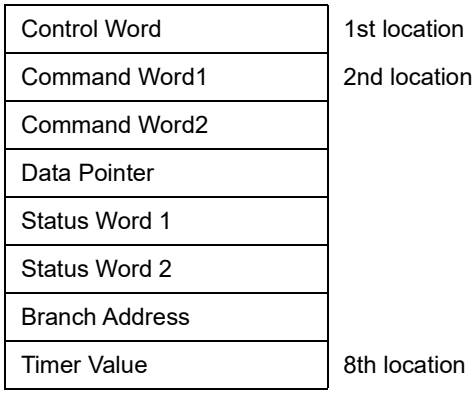

Figure 3-3 BC Command Block Architecture

The host must initialize each of the locations associated with each Command Block. The exception is for the two status locations that will be updated as Command Words are transmitted and corresponding Status Words are received. Command Blocks may be linked together in such a manner as to allow the generation of Major and Minor message frames. In addition, the BC can detect the assertion of Status Word bits and generate interrupts or branch to a new message frame, depending of course, on the specific conditions that arise.

3.3.1 Control Word

The first memory location of each BC Mode Command Block contains the Control word. Each control word contains the opcode, retry number, bus definition, RT-to-RT instruction, condition codes, and the block access message error. The control word is defined below:

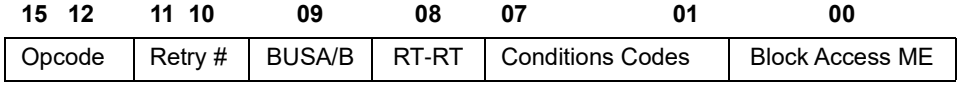

Figure 3-4 Control Word Definition

Bit	Bit Name	Description
12-15	**Opcode**	These bits define the opcode to be used by the module for that particular Command Block. If the opcode does not perform any 1553 function, all other bits are ignored. Each of the available opcodes is defined in section **3.3.1.1 OPCODE DEFINTION** on page 3-12
10-11	**Retry Number**	These bits define the number of retries for each individual Command Block and if retry opcode is used. If the Ping-Pong Enable Bit (bit 02 of the Control Register) is not enabled, all retries will occur on the programmed bus. However, if bit 02 is enabled, the first retry will always occur on the alternate bus, the second retry will occur on the primary bus, the third retry will occur on the alternate bus, and the fourth retry will occur on the primary bus. **Bit 11 / Bit 10 / No. of Retries** 0 / 1 / 1 1 / 0 / 2 1 / 1 / 3 0 / 0 / 4
09	**Bus A/B**	This bit defines on which of the two buses the command will be transmitted (i.e., primary bus). (Logic 1 = Bus A, Logic 0 = Bus B).
08	**RT-RT Transfer**	This bit defines whether or not the present Command Block is an RT-to-RT transfer and if the module should transmit the second command word. Data associated with an RT-to-RT is always stored by the module.
01-07	**Condition Codes**	These bits define the condition code the module uses for that particular Command Block. Each of the available condition codes is defined in section **3.3.1.2 BC CONDITION CODES** on page 3-14
00	**Block Access Message Error**	The module sets this bit to 1, indicating a protocol message error occurred in the RT's response. For this occurrence, the module will overwrite this bit prior to storing the Control Word into memory. An example of this type of error would be noise on the 1553 bus.

Control Word Description

3.3.1.1 OPCODE DEFINTION

Opcode	Field Name	Definition
0000	**End Of List**	This opcode instructs the module that the end of the command block has been encountered. Command processing stops and the interrupt is generated if the interrupt is enabled. No command processing takes place (i.e., no 1553).
0001	**Skip**	This opcode instructs the module to load the message-to-message timer with the value stored in timer value location. The module will then wait the specific time before proceeding to the next command block. This opcode allows for scheduling a specific time between message execution. No command processing takes place (i.e., no 1553).
0010	**Go To**	This opcode instructs the module to “go to” the command block as specified in the branch address location. No command process takes place (i.e., no 1553).
0011	**Built-in Test**	This opcode instructs the module to perform an internal built-in test. If the module passes the built-in test, then processing of the next command block will continue. However, if the module fails the built-in test, then processing stops. No command processing takes place (i.e., no 1553).
0100	**Execute Block; Continue**	This opcode instructs the module to execute the current command block and proceed to the next command block. This opcode allows for continuous operations.
0101	**Execute Block; Branch**	This opcode instructs the module to execute the current command block and unconditionally branch to the location as specified in the branch address location.
0110	**Execute Block; Branch on Condition**	This opcode instructs the module to execute the current command block and branch only if the condition is met. If no conditions are met, the opcode appears as an execute and continue.
0111	**Retry on Condition**	This opcode instructs the module to perform automatic retries, as specified in the control word, if particular conditions occur. If no conditions are met, the opcode appears as an execute and continue.
1000	**Retry on Condition; Branch**	This opcode instructs the module to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met, the module retries. Once all retries have executed, the module branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and branch.
1001	**Retry on Condition; Branch if all Retries Fail**	This opcode instructs the module to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met and all the retries fail, the module branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and continue.
1010	**Interrupt; Continue**	This opcode instructs the module to interrupt and continue processing on the next command block. When using this opcode, no 1553 processing occurs.

Opcode Definition

Opcode	Field Name	Definition
1011	**Call**	This opcode instructs the module to “go to” the command block as specified in the branch address location without processing this block. The next command block address is saved in an internal register so that the module may remember one address and return to the next command block. No command processing takes place (i.e., no 1553).
1011	**Call**	This opcode instructs the module to “go to” the command block as specified in the branch address location without processing this block. The next command block address is saved in an internal register so that the module may remember one address and return to the next command block. No command processing takes place (i.e., no 1553).
1100	**Return to Call**	This opcode instructs the module to return to the command block address saved during the Call opcode. No command processing takes place (i.e., no 1553).
1101	**Reserved**	The module will generate an illegal opcode interrupt (if interrupt enabled) and automatically stop execution if a reserved opcode is used.
1110	**Load Minor Frame Timer**	This opcode instructs the module to load the minor frame timer (MFT) with the value stored in the eighth location of the current command block. The timer will be loaded after the previous MFT has decremented to zero. After the MFT timer is loaded with the new value, the module will proceed to the next command block. No command processing takes place (i.e., no 1553).
1111	**Return to Branch**	This opcode instructs the module to return to the command block address saved during a Branch opcode. No command processing takes place (i.e., no 1553).

Opcode Definition (Continued)

Note For entries with interrupts enabled, all interrupts are logged after message processing is completes.

3.3.1.2 BC CONDITION CODES

Condition codes have been provided as a means for the *M8K1553MCH* to perform certain functions based on the RT's Status Word. In an RT-to-RT transfer, the conditions apply to both of the Status Words. Each bit of the condition codes is defined below.

Bit Number	Description
07	Message Error. This condition will be met if the module detects an error in the RT's response, or if it detects no response. The module will wait 15 μsec. in 1553B mode and 9 μsec. in 1553A mode before declaring an RT no response (see section **3.6 MIL-STD-1553A/B Operation: BC Mode** on page 3-18).
06	Status Word Response with the Message Error bit set (Bit time 09 in 1553A mode). This condition is met if the module detects that the RT's Status Word has the Message Error bit set.
05	Status Word Response with the Busy bit set (Bit time 16 in 1553A mode). This condition is met if the module detects that the RT's Status Word has the Busy bit set.
04	Status Word Response with the Terminal Flag bit set (Bit time 19 in 1553A mode). This condition is met if the module detects that the RT's Status Word has the Terminal Flag bit set.
03	Status Word Response with the Subsystem Fail bit set (Bit time 17 in 1553A mode). This condition is met if the module detects that the RT's Status Word has the Subsystem Fail bit set.
02	Status Word Response with the Instrumentation bit set (Bit time 10 in 1553A mode). This condition is met if the module detects that the RT's Status Word has the Instrumentation bit set.
01	Status Word Response with the Service Request bit set (Bit time 11 in 1553A mode). This condition is met if the module detects that the RT's Status Word has the Service Request bit set.

Condition Codes

3.3.2 1553 Command Words

The next two locations of the BC Mode Command Block are for 1553 Command Words. In most 1553 messages, only the first Command Word needs to be initialized. However, in an RT-to-RT transfer, the first Command Word is the Receive Command and the second Command Word is the Transmit Command.

3.3.3 Data Pointer

The fourth location of the BC Mode Command Block is the data pointer that points to the first memory location to store or retrieve the Data Words associated with the message for that command block. This data structure allows the module to store or retrieve the exact specified number of Data Words, thus saving memory space and providing efficient space allocation.

Note In an RT-to-RT transfer, the module uses the data pointer as the location in memory to store the transmitted data in the transfer.

One common application for the data pointer occurs when the module needs to send the same data words to several RTs. Here, each Command Block associated with those messages would contain the same data pointer value, and, therefore, retrieve and transmit the same data. Note that the Data Pointer is never updated (i.e., the module reads and writes the pointer but never changes its value).

3.3.4 1553 Status Words

The next two locations in the BC Mode Command Block are for Status Words. As the RT responds to the BC's command, the corresponding Status Word will be stored in Status Word 1. In an RT-to-RT transfer, the first Status Word will be the status of the Transmitting RT while the second Status Word will be the status of the Receiving RT.

3.3.5 Branch Address

The seventh location in the BC Mode Command Block contains the starting location of the branch. This location simply allows the module to branch to another location in memory when certain opcodes are used.

3.3.6 Timer Value

The last location in the BC Mode Command Block is the Timer Value. This timer is used:

- To set up minor frame schedules when using the Load Minor Frame Timer opcode (1110). The MFT counter is clocked by a 15.625 KHz. (64 µsec.) internal clock. The MFT counter runs continuously during message processing and must decrement to zero prior to loading the next Minor Frame time value.
- As a message-to-message timer (MMT) when using the Skip opcode (0001). The MMT timer is clocked at the 24 MHz (41.666 nsec.) rate and allows for scheduling of specific time between message execution.

3.4 Command Block Chaining

To determine the first Command Block, set the initial start address in the Command Block Pointer Register [Address 0010 (H)]. The Command Blocks will execute in a contiguous fashion as long as no “go to”, “branch”, “call”, or “return” opcodes are used. With the use of these opcodes, almost any memory configuration is possible. Figures 3-5 and 3-6 show how several Command Blocks may be linked together to form a command frame and how branch opcodes may be used to link minor frames. The minimum BC intermessage gap is 28.0 µsec.

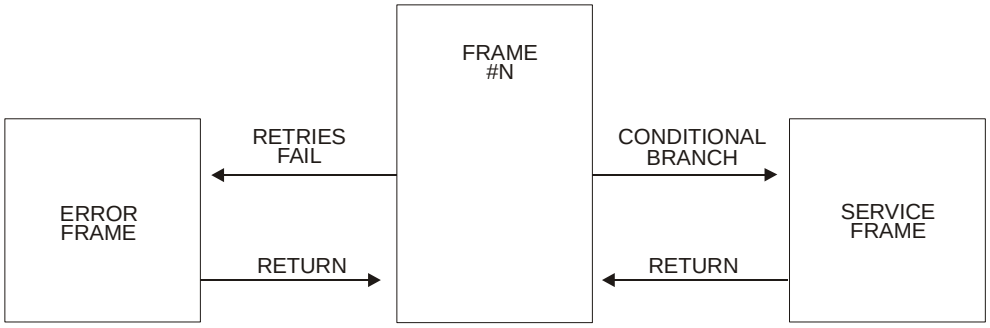

Figure 3-5 Message Control Options

The example in Figure 3-6 shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each minor frame goes out at 10 msec. (100Hz). If each minor frame is 10 µsec. long, Message A is sent every 10 msec., Message B is sent every 20 µsec., and Message C is sent every 40 µsec.

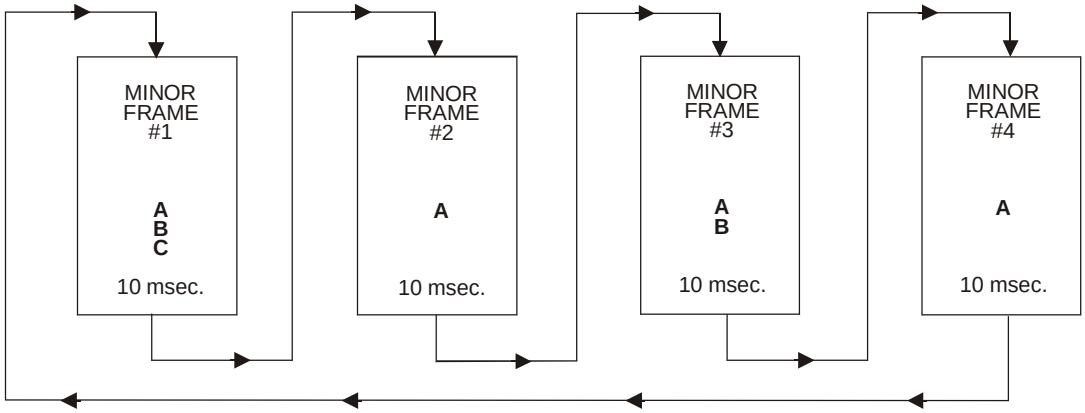

Figure 3-6 Minor Frame Sequencing

3.5 Memory Architecture

After reviewing the control registers, it is advantageous to look at how to set up memory to configure the *M8K1553MCH* as a Bus Controller. This section shows one method for defining the memory configuration.

The configuration shows the Command Blocks, data locations, and the Interrupt Log List as separate entities. Figure 3-7 shows that the first block of memory is allocated for the Command Blocks. Notice that the Command Block Pointer Register initially points to the control word of the first Command Block. After completing execution of that first Command Block, the Command Block Pointer Register will automatically be updated to show the address of the next Command Block.

Following the Command Block locations is the memory required for all the data words. In BC applications, the number of data words for each Command Block is known. In Figure 3-7, for example, the first Command Block has allocated several memory locations for expected data. Conversely, the second Command Block has only allocated a few memory locations. Since the number of data words associated with each Command Block is known, memory may be used efficiently.

Also shown as a separate memory area is the Interrupt Log List (see **Interrupt Log List Pointer Register** on page 3-8). Notice that the Interrupt Log List Pointer Register points to the top of the initial Log List. After execution of that first BC Command Block, the Interrupt Log List Pointer Register will automatically be updated if interrupt condition exists.

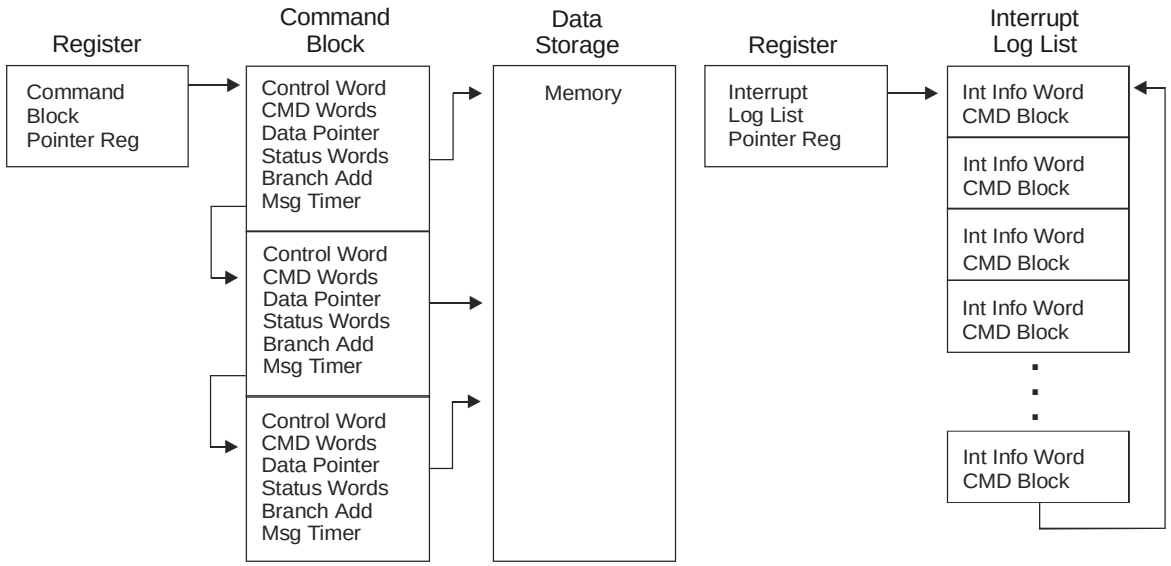

Figure 3-7 Memory Architecture for BC Mode

3.6 MIL-STD-1553A/B Operation: BC Mode

To maximize flexibility, the *M8K1553MCH* can operate in many different systems that use various protocols. Specifically, two of the protocols that the module may be used with are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, configure the module through the Control register (ERTO Bit 09) and the Operational Status register (A/B_STD Bit 07). Table 3-1 defines the four ways to program the *M8K1553MCH*.

A/B_STD	ERTO	RESULT
0	0	1553B standard, 1553B response (in 14 μsec.)
0	1	1553B standard, extended response (in 30 μsec.)
1	0	1553A standard, 1553A response (in 9 μsec.)
1	1	1553A standard, extended response (in 21 μsec.)

Table 3-1 MIL-STD-1553A/B Operation: BC Mode

When configured as a MIL-STD-1553A bus controller, the module will operate as follows:

- Looks for the RT response within 9 μsec.
- Defines all mode codes without data
- defines subaddress 00000 as a mode code

4 Remote Terminal Operation

Chapter 4 describes *M8K1553MCH* operation in Remote Terminal (RT) mode. The topics covered in this chapter are:

Note The *M8K1553MCH* can be configured both as a Remote Terminal and as a Bus Monitor. For more information about this feature see section **5.6 RT/ Concurrent Monitor Operation** on page 5-15.

4.1 Control Registers

The Control registers are read/write unless otherwise stated. All Control registers must be accessed in Word mode. All Control register bits are active high and are reset to 0 unless otherwise stated.

Figure 4-1 below illustrates the Control registers for Remote Terminal mode.

Illegalization Registers (16 registers)	0020-003E H
Reserved	0014-001E H
1553 Status Word Bits Register	0012 H
RT Descriptor Pointer Register	0010 H
Time Tag Register	000E H
BIT Word Register	000C H
Interrupt Log List Pointer Register	000A H
Pending Interrupt Register	0008 H
Interrupt Mask Register	0006 H
Current Command Block Register	0004 H
Operational Status Register	0002 H
Control Register	0000 H

Figure 4-1 Control Registers Map: RT Mode

4.1.1 Control Register

Address: 0000 (H)
Read/Write

Use the Control register to configure the module for RT operation. To make changes to the RT mode and this register, the STEX bit (Bit 15) must be logic 0.

Bit	Bit Name	Description
15	**STEX**	Start Module Execution 1 = Initiates module operation. 0 = Inhibits module operation. A remote terminal address parity error prevents RT Mode operation regardless of the logical state of this bit. If an RT address parity error exists, bit 03 of the Operational Status Register will be set low and bit 02 of the Operational Status Register will be set high.
14	**SBIT**	Start Module BIT 1 = Places the module into the Built-In Test routine. The BIT routine takes 1 msec. to execute and has a fault coverage of 93.4%. If the module has been started, the host must halt the module in order to place the module into the Built-In Test mode (STEX = 0). **Note** If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, SBIT has priority.
13	**Reserved**	Set to 0
12	**BUAEN**	Bus A Enable 1 = Enables Bus A operation. 0 = The module does not recognize Commands received over Bus A.
11	**BUBEN**	Bus B Enable 1 = Enables Bus B operation. 0 = The module does not recognize Commands received over Bus B.
10	**Reserved**	Set to 0
09	**PPACK**	Ping-Pong Acknowledge. This read-only bit acknowledges the Ping-Pong operation. The Ping-Pong Enable is acknowledged by transitioning from a logical zero to a logical one, while the Ping-Pong Disable is acknowledged by transitioning from a logical one to a logical zero.
07-08	**RTM[1-0]**	Remote Terminal Mode bits. These two bits determine the RT mode of operation. **RTM[1—0] RT Mode** 0 0 Mode #0 Index or Ping-pong operation 0 1 X Reserved 1 0 Mode #1 Circular buffer 1 operation 1 1 Mode #2 Circular buffer 2 operation
05-06	**Reserved**	Set to 0
04	**BCEN**	Broadcast Enable 1 = Enables the broadcast option for RT Mode. 0 = Enables remote terminal address 31 as a unique remote terminal address.

Control Register

Bit	Bit Name	Description
03	**DYNBC**	Dynamic Bus Control Acceptance. This bit controls the module's ability to accept the dynamic bus Control mode code. 1 = Allows the module to respond to a dynamic bus Control mode code with status Word bit 18 set to a logic one. 0 = Prevents the assertion of status Word bit 18 upon reception of the dynamic mode code.
02	**PPEN**	Ping-Pong Enable 1 = Enables the ping-pong buffer feature of the module and disables the message indexing feature. 0 = Disables the ping-pong feature and enables the message indexing feature.
01	**INTEN**	Interrupt Log Enable 1 = Enables the interrupt logging feature. 0 = Prevents the logging of interrupts.
00	**XMTSW**	Transmit Last Status Word 1 = Allows the module to automatically execute the Transmit Status Word mode code when configured for MIL-STD-1553A mode operation.

Control Register (Continued)

4.1.2 Operational Status Register

Address: 0002 (H)
Read/Write

The Operational Status register provides pertinent status information for RT Mode and is not reset to 0000 H on reset. Instead the bits A/B_STD, and RTA[4-0] are set to 1.

Bit	Bit Name	Description
11-15	**RTA[4-0]**	Remote Terminal Address Bits. These five bits contain the remote terminal address. The RTA4 bit is the MSB bit, while the RTA0 bit is the LSB bit.
10	**RTAPTY**	Terminal Address Parity Bit. This bit is appended to the remote terminal address bus (RTA[4-0]) to supply odd parity. The module requires odd parity for proper operation.
09	**MSEL1**	Mode Select 1. In conjunction with Mode Select 0, this bit determines the module's mode of operation.
08	**MSEL0**	Mode Select 0. In conjunction with Mode Select 1, this bit determines the module's mode of operation.
		MSEL1 / **MSEL0** / **Mode Of Operation** 0 / 0 / BC Mode 0 / 1 / RT Mode 1 / 0 / BM Mode 1 / 1 / RT/Concurrent Monitor mode
07	**A/B_STD**	Military Standard 1553A or 1553B. This bit determines whether the module will operate under MIL-STD-1553A or 1553B protocol. 1 = Enables the XMTSW bit (Bit 00 of the Control Register) (1553A). 0 = Automatically allows the module to operate under the MIL-STD-1553B protocol.
04-06	**Reserved**	These read-only bits are not applicable.
03	**EX**	module Executing. This read-only bit indicates whether the module is presently executing or is idle. 1 = The module is executing. 0 = The module is idle.
02	**TAPF**	Terminal Address Parity Fail. Read only. This bit indicates the observance of a terminal address parity error. The module checks for odd parity. This bit reflects the parity of Operational Status Register bits 10-15.
01	**READY**	module Ready. This read-only bit is cleared on reset. 1 = The module has completed initialization or BIT, and regular operation may begin.
00	**TERACT**	module Terminal Active. This read-only bit is cleared on reset. 1 = The module is presently processing a 1553 message.

Operational Status Register

Note
1. Remote Terminal Address and Parity are checked on start of execution
2. To make changes to the RT Mode and this register, the STEX bit (Bit 15 in the Control Register) must be logic 0.

4.1.3 Current Command Block Register

Address: 0004 (H)
Read only

This 16-bit register contains the last valid 1553 Command processed by the module.

Bit	Bit Name	Description
00-15	**CC[15-0]**	Current Command. These bits contain the latest valid 1553 Command that was received by the module. This register is valid 13 μsec. after the TERACT bit (Bit 00 of the Operational Status Register) is set to 0.

Current Command Block Register

4.1.4 Interrupt Mask Register

Address: 0006 (H)
Read/Write

M8K1553MCH interrupt architecture allows for the masking of all interrupts. An interrupt is masked if the corresponding bit of this register is set to logic 0. This feature allows the host to temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event.

Bit	Bit Name	Description
12-15	**Reserved**	Set to 0
11	**MERR**	Message Error Interrupt
10	**SUBAD**	Subaddress Accessed Interrupt
09	**BDRCV**	Broadcast Command Received Interrupt
08	**IXEQ0**	Index Equal Zero Interrupt
07	**ILLCMD**	Illegal Command Interrupt
00-06	**Reserved**	Set to 0

Interrupt Mask Register

4.1.5 Pending Interrupt Register

Address: 0008 (H)
Read only

The Pending Interrupt Register is used to identify events that generate interrupts. The assertion of any bit in this register generates an interrupt. A register read of the Pending Interrupt Register will clear all bits.

Bit	Bit Name	Description
12-15	**Reserved**	Ignore on read.
11	**MERR**	Message Error Interrupt. 1 = A message error occurred. The module can detect Manchester, sync-field, Word count errors (too many or too few), MIL-STD-1553 Word parity, bit count errors (too many or too few), and protocol errors. If not masked, this bit is always set and an interrupt generated when the module asserts bit-time 9 (Message Error) of the 1553 status Word (e.g., illegal Commands, invalid Data Word, etc.).
10	**SUBAD**	Subaddress Accessed Interrupt. 1 = A pre-selected subaddress has transacted a message. To determine the exact subaddress, the host interrogates the interrupt log IAW.
09	**BDRCV**	Broadcast Command Received Interrupt. 1 = The module's receipt of a valid broadcast Command. The module suppresses status Word transmission.
08	**IXEQ0**	Index Equal Zero Interrupt. The module sets this bit to 1 to indicate the completion of a pre-defined number of Commands by the RT. Upon assertion of this interrupt, the host updates the subaddress descriptor to prevent the potential loss of data.
07	**ILCMD**	Illegal Command Interrupt. 1 = The module received an illegal Command. Upon receipt of this Command, the module responds with a status Word only; Bit-time 09 (Message Error) of the 1553 status Word is set to a logic 1.
00-06	**Reserved**	Ignore on read.

Pending Interrupt Register

4.1.6 Interrupt Log List Pointer Register

Address: 000A (H)
Read/Write

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts.

The *M8K1553MCH* architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K memory space. The lower 5 bits of this register should be initialized to a logic 0. The module controls the lower 5 bits to implement the ring-buffer architecture. Read this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Bit	Bit Name	Description
00-15	**ILLP[15-0]**	Interrupt Log List Pointer Bits. **Note** Bits 05-15 indicate the starting Base Address, while bits 00-04 indicate the ring location of the Interrupt Log List

Interrupt Log List Pointer Register

4.1.7 BIT Word Register

Address: 000C (H)
Read/Write

The BIT Word register contains information on the current status of the module hardware. The RT transmits the contents of the register upon reception of a Transmit BIT Word Mode Code.The user defines the lower 8 bits of this register.

Bit	Bit Name	Description
15	**DMAF**	DMA Fail. 1 = All the module's internal DMA activity was not completed within 16 μsec.
14	**WRAPF**	Wrap Fail. The module automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is set. The loopback path is via the MIL-STD-1553 bus transceiver.
13	**TAPF**	Terminal Address Parity Fail. This bit reflects the outcome of the remote terminal address parity check. 1 = A parity failure. When a parity error occurs the module does not begin operation (STEX bit forced to a logic 0) and bus A and B do not enable.
12	**BITF**	BIT Fail. 1 = A BIT failure. Interrogate bits 11 through 08 to determine the specific failure.
11	**BUAF**	Bus A Fail. 1 = A BIT test failure in Bus A.
10	**BUBF**	Bus B Fail. 1 = A BIT test failure in Bus B.
09	**MSBF**	Memory Test Fail. Most significant memory byte failure.
08	**LSBF**	Memory Test Fail. Least significant memory byte failure.
00-07	**UDB[7-0]**	User-Defined Bits.

BIT Word Register

4.1.8 Time Tag Register

Address: 000E (H)
Read Only

The Time Tag register reflects the state of a 16-bit free running counter. The resolution of this counter is 64ìsec./bit. The Time Tag counter is automatically reset when the module receives a valid synchronize without Data mode code. The module automatically loads the Time Tag counter with the data associated with reception of a valid synchronize with Data mode code.

The Time Tag counter begins operation in one of two cases:

- *Either* within 64 µsec. of the rising (final) edge of a reset
- *Or* the receipt of one of the following valid mode codes:
  - reset of the remote terminal
  - sync with/without data

When the module is halted (STEX bit 15 in the Control register = 0), the Time Tag continues to run.

Bit	Bit Name	Description
00-15	**TT[15-0]**	Time Tag Counter Bits.

Time Tag Register

4.1.9 RT Descriptor Pointer Register

Address: 0010 (H)
Read/Write

Each subaddress and mode code has a reserved block of memory containing information about how to process a valid Command to that subaddress or mode code. Located contiguously in memory, these reserved memory locations are called a descriptor space. The RT Descriptor Pointer register contains an address that points to the top of this memory space. The module uses the T/R bit, subaddress/mode code field, and mode code to select one block in the descriptor table for message processing. The RT Descriptor Pointer register is static during message processing.

Bit	Bit Name	Description
00-15	**RTDA[15-0]**	RT descriptor Address Bits

RT Descriptor Pointer Register

4.1.10 1553 Status Word Bits Register

Address: 0012 (H)
Read/Write

The 1553 Status Word Bits register controls the outgoing MIL-STD-1553 Status Word. The host controls the Instrumentation, Busy, Terminal Flag, Service Request, and Subsystem Flag by writing to bits 09 through 00 of this register. The module's Status Word response reflects assertion of these bit(s) until negated by the host unless the Immediate Clear Function is enabled. The Immediate Clear Function automatically clears these bits after being transmitted in a Status Word.

The Immediate Clear Function does not affect the operation of the Transmit Last Status Word and Transmit Last Command Word Mode Codes. Transaction of a legal valid Command with the INS bit set to a logic one and the Immediate Clear Function enabled, results in the transmission of a 1553 Status Word with bit 10 asserted. If the ensuing Command is a Transmit Last Status Word or Last Command mode code, bit 10 of the outgoing 1553 Status Word remains a logic 1.

For MIL-STD-1553B applications, the 1553 Status Word Bits register is as follows:

Bit	Bit Name	Description
15	**IMCLR**	Immediate Clear Function. 1 = Enables the Immediate Clear Function (IMF) of the module. Enabling the IMF results in the clearing of the INS, BUSY, TF, SRQ, and/or SUBF bit immediately after a message is completed. To enable this function, set this bit to 1 when setting bit(s) INS, BUSY, TF, SRQ, and/or SSYSF to 1. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
10-14	**Reserved**	Set to 0
09	**INS**	Instrumentation Bit. This bit sets the Instrumentation bit of the MIL-STD-1553B Status Word. (Bit 10 of the Status Word).
08	**SRQ**	Service Request Bit. This bit sets the Service Request bit of the MIL-STD-1553B Status Word. (Bit 11 of the Status Word).
04-07	**Reserved**	Set to 0
03	**BUSY**	Busy Bit. Assertion of this bit is reflected in the outgoing MIL-STD-1553B Status Word. 1 = Prevents memory accesses. (Bit 16 of the Status Word).
02	**SSYSF**	Subsystem Flag Bit. This bit sets the Subsystem Flag bit of the MIL-STD-1553B Status word. (Bit 17 of the Status Word).
01	**Reserved**	Set to 0
00	**TF**	Terminal Flag. Assertion of this bit is reflected in the outgoing MIL-STD-1553B Status Word. The module automatically sets this bit if a BIT failure occurs. Inhibit Terminal Flag mode code prevents the assertion by the host. Override Inhibit Terminal Flag Mode Code re-establishes the Terminal Flag option. (Bit 19 of the Status Word).

1553 Status Word Bits Register: MIL-STD-1553B

For MIL-STD-1553A applications, the 1553 Status Word Bits register

Bit	Bit Name	Description
15	**IMCLR**	Immediate Clear Function. 1 = Enables the Immediate Clear Function (IMF) of the module. Enabling the IMF results in the clearing of the bits 10-19 immediately after a Status Word is transmitted. To enable this function, set this bit when writing to bits 10-19. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
10-14	**Reserved**	Set to 0
09	**SB10**	Status bit time 10
08	**SB11**	Status bit time 11
07	**SB12**	Status bit time 12
06	**SB13**	Status bit time 13
05	**SB14**	Status bit time 14
04	**SB15**	Status bit time 15
03	**SB16**	Status bit time 16
02	**SB17**	Status bit time 17
01	**SB18**	Status bit time 18
00	**SB19**	Status bit time 19

1553 Status Word Bits Register: MIL-STD-1553A

4.1.11 Illegalization Registers

Address: 0020 – 003E (H)

The 16 registers are divided into eight blocks, two registers per block, as shown in Table 4-1:

Block Name	Address (H)
Receive	0020 and 0022
Transmit	0024 and 0026
Broadcast Receive	0028 and 002A
Broadcast Transmit (Automatically Illegalized)	002C and 002E
Mode Code Receive	0030 and 0032
Mode Code Transmit	0034 and 0036
Broadcast Mode Code Receive	0038 and 003A
Broadcast Mode Code Transmit	003C and 003E

Table 4-1: Illegalization Register Blocks

The blocks correspond to the following types of Commands. Register address 0020 (H) and 0022 (H) illegalize receive Commands to 32 subaddresses. The most significant bit of register 0020 (H) controls the illegalization of subaddress 01111. The least significant bit controls subaddress 00000. Register 0022 (H) controls

illegalization of subaddresses 10000 through 11111. The least significant bit relates to subaddress 10000; the most significant bit relates to subaddress 11111. Transmit Commands and Broadcast Commands (both receive and transmit) use the same encoding scheme as receive subaddress illegalization.

Register 0030 (H) through 003E (H) controls the illegalization of mode codes. Register 0030 (H) governs the illegalization of receive mode codes (T/R bit = 0) 00000 through 01111 and register 0032 (H) mode codes 10000 through 11111. Register blocks Transmit Mode Code (T/R bit = 1), Broadcast Receive Mode Codes, and Broadcast Transmit Mode Codes use the same decode scheme as receive mode codes.

Table 4-2 shows the illegalization register map. For Receive, Transmit, Broadcast Receive, and Broadcast Transmit blocks, the numbers shown in the column under each bit number identify the specific subaddress or mode code (in hex) that the register bit illegalizes (Logical 0 = legal, Logical 1 = illegal).

Name	Register Address (H)																
Bit #		15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Receive	0020	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0022	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Transmit	0024	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0026	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Broadcast Receive	0028	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	002A	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Broadcast Transmit	002C	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
	002E	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
Mode Code Receive	0030	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0032	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Code Transmit	0034	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0036	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Broadcast Receive	0038	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	003A	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Broadcast Transmit	003C	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	003E	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY

Table 4-2: Illegalization Register Map

1. XX = Automatically illegalized by the module.
2. YY = Automatically illegalized by the module in 1553B only.
3. ZZ = Automatically illegalized by the module in 1553B and 1553A if XMTSW is enabled.
4. WW = Automatically illegalized in 1553A.
5. UU = Automatically illegalized in 1553A if XMTSW enabled.

4.2 Descriptor Block

To process messages, the module uses data from the Control Registers with data stored in the RAM. The module accesses a 4-word descriptor block stored in RAM. The descriptor block is accessed at the beginning and end of Command processing. Multiple descriptor blocks are sequentially entered into memory to form a descriptor table. The following paragraphs discuss the descriptor block in detail.

The host controlling the module allocates 512 consecutive memory spaces for the subaddress and mode code Descriptor Table (see Figure 4-2 on page 4-14). The top of the Descriptor Table can reside at any address location. The Control registers are linked to the descriptor table via the Descriptor Address Register contents. Each descriptor block contains a Control Word, Data Pointer A, Data Pointer B, and Broadcast Data Pointer. Each subaddress and mode code is assigned a descriptor for receive and transmit Commands (T/R bit equals 0 or 1.).

Control Word information allows the module to generate interrupts, buffer messages, and control message processing. For a receive Command, the Data List Pointer is read to determine the top of the data buffer. The module stores data sequentially from the top of data buffer plus two locations (e.g., 0100H, 0102H, 0104H, 0106H, etc.). When processing a transmit Command, the Data List Pointer is read to determine where Data Words are retrieved. The module retrieves Data Words sequentially from the address the Data List Pointer designates plus two 16-bit address locations.

The Broadcast Data Pointer allows for separate storage of non-broadcast data from broadcast data per MIL-STD-1553B Notice II. The user enables or disables this feature via the Control Word's least significant bit. When disabled, the non-broadcast and broadcast data is stored via Data List Pointer A or B. For transmit Commands, the Broadcast Data Pointer is not used. The module does not transmit any information on the receipt of a broadcast transmit Command.

The module reads the descriptor block during Command processing (i.e., after assertion of TERACT). The module reads the Control Word and three Data Pointers. The module then begins the acquisition of Data Words for either transmission or storage.

After transmission or reception, the module begins post-processing. The Descriptor Block is updated. An optional interrupt log entry is performed after a descriptor update. During the descriptor update, the module modifies the Control Word index field and bits 4, 2, and 1, if required. The module updates Data Pointer A if no message errors occurred during the message transaction. Reception of a broadcast Command, with no message errors, results in the update of the Broadcast Data Pointer. Neither Data Pointer A or B is updated if the module has the ping-pong mode of operation enabled.

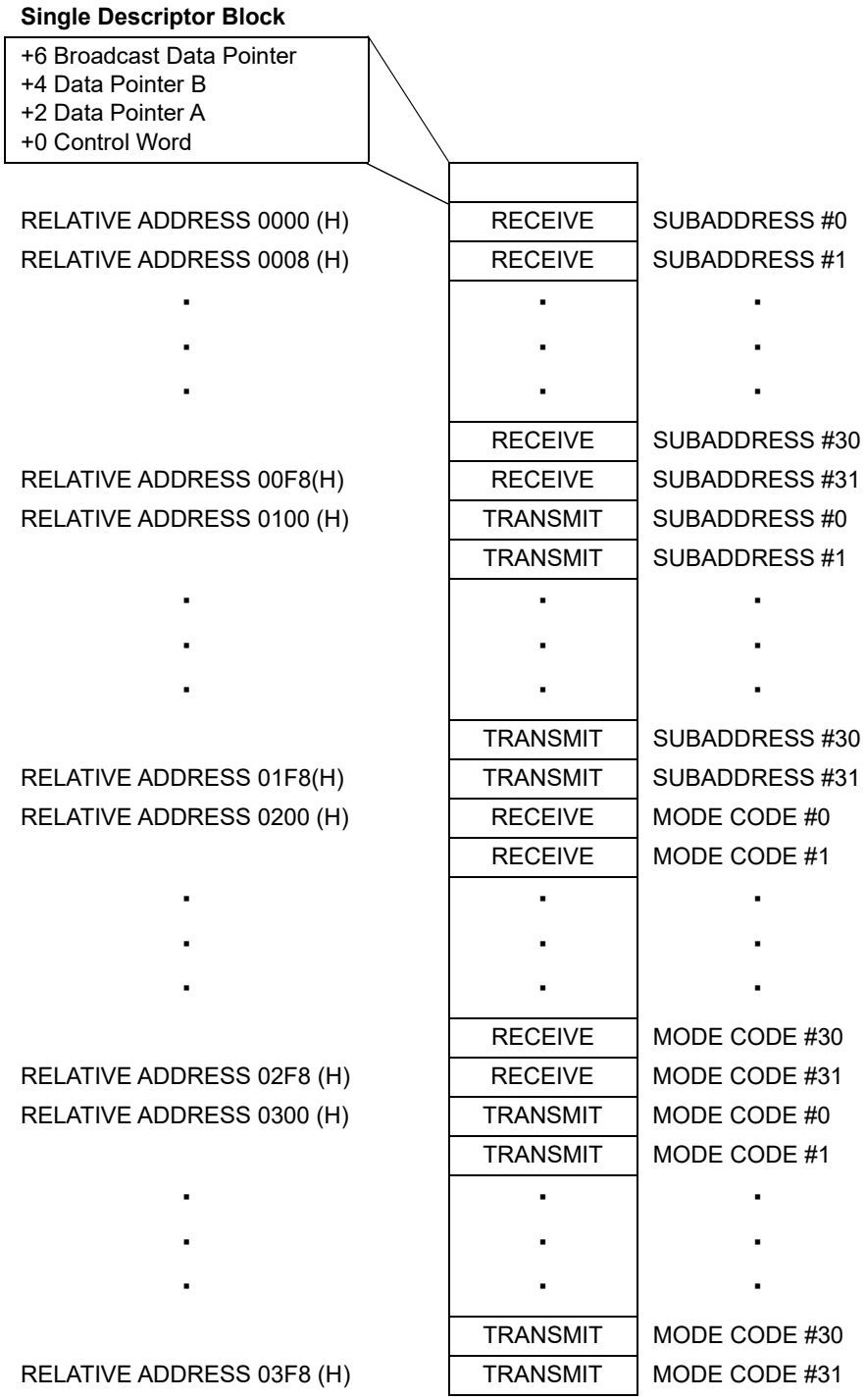

Figure 4-2 Descriptor Table

4.2.1 Receive Control Word

Information contained in the Receive Control Word assists the module in message processing. The following bits describe the receive subaddress descriptor Control Word. The descriptor Control Word is initialized by the host and updated by the module during Command post-processing.

Bit	Bit Name	Description
08-15	**INDX**	Index Field. These bits define multiple message buffer length. The host uses this field to instruct the module to buffer *N* messages. *N* can range from 0 (00 H) to 256 (FF H). If buffer ping-ponging is enabled, the INDX field is 'don't care' (i.e., does not contain applicable information). During ping-pong mode operation, you should initialize the index field to 00 (H). The RT does not perform multiple message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the subaddress is illegalized. The module can generate an interrupt when the index field transitions from one to zero (see bit 07).
07	**INTX**	Interrupt Index Equals Zero. 1 = Enables the generation of an interrupt when the index field transitions from 1 to 0. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
06	**IWA**	Interrupt When Accessed. 1 = Enables the generation of an interrupt when the subaddress receives a valid Command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	**IBRD**	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when the subaddress receives a valid broadcast Command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	**BAC**	Block Accessed. The host initializes this bit to zero; the module overwrites the zero with a logic one upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	**Reserved**	Set to 0
02	**A/B**	Buffer A/B. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a 'don't care' if buffer ping-ponging is not enabled.
01	**BRD**	Broadcast Received. 1 = Reception of a valid broadcast Command.
00	**NII**	Notice II. 1 = Enables the use of the Broadcast Data Pointer as a buffer for Broadcast Command information. 0 = Broadcast information is stored in the same buffer as non-broadcast information.

Receive Control Word

4.2.2 Transmit Control Word

Information contained in the Transmit Control Word assists the *M8K1553MCH* in message-processing. The following bits describe the transmit subaddress descriptor Control Word. The descriptor control Word is initialized by the host and updated by the module during Command post-processing.

Bit	Bit Name	Description
07-15	**Reserved**	Set to 0
06	**IWA**	Interrupt When Accessed. 1 = Enables the generation of an interrupt when the subaddress receives a valid Command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	**Reserved**	Set to 0
04	**BAC**	Block Accessed. The host initializes this bit to zero; the module overwrites the zero with a logic one upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	**Reserved**	Set to 0
02	**A/B**	Buffer A/B. Indicates the Data pointer to access when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a ‘don’t care’ if buffer ping-ponging is not enabled.
01	**BRD**	Broadcast Received. 1 = Reception of a Broadcast Command.
00	**Reserved**	Set to 0

Transmit Control Word

4.2.3 Mode Code Receive Control Word

Information contained in the Mode Code Receive Control Word assists the *M8K1553MCH* in message processing. The following bits describe the receive mode code descriptor Control Word. The descriptor control Word is initialized by the host and updated by the module during Command postprocessing.

Note In MIL-STD-1553A, all mode codes are without data, and the T/R bit is ignored.

Bit	Bit Name	Description
08-15	**INDX**	Index Field. These bits define multiple message buffer length. The host uses this field to instruct the module to buffer *N* messages. *N* can range from 0 (00 H) to 256 (FF H). If buffer ping-ponging is enabled, the INDX field is 'don't care' (i.e., does not contain applicable information). The module does not perform message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the mode code is illegalized. The module can generate an interrupt when the index field transitions from one to zero (see bit 07).
07	**INTX**	Interrupt Index Equals 0. 1 = Enables the generation of an interrupt when the index field transitions from 1 to 0. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
06	**IWA**	Interrupt When Accessed. 1 = Enables the generation of an interrupt when mode code Command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	**IBRD**	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when a valid broadcast mode code Command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	**BAC**	Block Accessed. The host initializes this bit to zero; the module overwrites the zero with a logic 1 upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	**Reserved**	Set to 0
02	**A/B**	Buffer A/B. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, you designate the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a 'don't care' if buffer ping-ponging is not enabled.
01	**BRD**	Broadcast Received. 1 = Reception of a valid broadcast Command.
00	**NII**	Notice II. 1 = Enables the use of the Broadcast Data Pointer as a buffer for broadcast Command information. 0 = Broadcast information is stored in the same buffer as non-broadcast information.

Mode Code Receive Control Word

4.2.4 Mode Code Transmit Control Word

Information contained in the Mode Code Transmit Control Word assists the *M8K1553MCH* in message processing. The following bits describe the transmit mode code descriptor Control Word. You initialize the descriptor Control Word and the module updates it during Command post-processing.

Note In MIL-STD-1553A, all mode codes are without data, and the T/R bit is ignored.

Bit	Bit Name	Description
07-15	**Reserved**	Set to 0
06	**IWA**	Interrupt When Accessed. 1 = Enables the generation of an interrupt when mode code Command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	**IBRD**	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when a broadcast mode code is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	**BAC**	Block Accessed. The host initializes this bit to 0; the module overwrites the 0 with a logic 1 upon completion of message processing. Upon reading a 1, the host resets this bit to 0 in preparation for the next message.
03	**Reserved**	Set to 0
02	**A/B**	Buffer A/B. This bit indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, you designate the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a ‘don’t care’ if buffer ping-ponging is not enabled.
01	**BRD**	Broadcast Received. 1 = Reception of a broadcast Command.
00	**Reserved**	Set to 0

Mode Code Transmit Control Word

4.2.5 Data Pointer A and B (Mode #0)

Data List Pointer A and B contains address information for the retrieval and storage of message Data Words. In the index mode of operation, the module reads Data Pointer A to determine the location of data for retrieval or storage. The module uses the Data Pointer to initialize an internal counter, which increments after each Data Word. For a receive Command, the module stores the incoming Data Word sequentially into memory. As part of Command post-processing, the module writes a new Data pointer into the descriptor block. The module continues to update the Data pointer until the Control Word index field decrements to zero. An example is shown in Figure 4-3.

Note The index feature is not applicable for transmit Commands (i.e., T/R bit = 1).

Bit	Bit Name	Description
00-15	**DP[15-0]**	Data Pointer Bits. The second and third Words of the descriptor block contain the data buffer location. The module accesses either Data Pointer A or Data Pointer B depending on the state of Control Word Bit 02 during ping-pong operation. For index operation, the module accesses only Data Pointer A. The module updates Data pointer A after message processing is complete and the index field is not equal to zero and ping-pong operation disabled. Bit 15 is the most significant bit; bit 00 is the least significant bit.

Data Pointer A and B

For ping-pong buffer operation, the host uses either Data Pointer A or Data Pointer B. The module determines which pointer to access via the state of Control Word bit 02. The module retrieves or stores Data Words from the address contained in the Data pointer, automatically incrementing the Data Pointer as Data Words are received. The Data pointer is never updated as part of Command postprocessing in the ping-pong mode of operation. See Figures 4-4 and 4-5.

Receive Address	CONTROL WORD	Index Field Contents 03xx (H)
# Descriptor Block	DATA POINTER A	Data Pointer A: 0100 (H)
	DATA POINTER B	Data Pointer B: Xxxx (H)
	BROADCAST DATA POINTER	Broadcast Data Pointer: Xxxx (H)
Command #1 Receive three words	Message Info Word	0200 (H) Index equals three
	Time Tag	0202 (H)
	Data Word #1	0204 (H)
	Data Word #2	0206 (H)
	Data Word #3	0208 (H) Index decrements two
Command #2 Receive two words	Message Info Word	020A(H) Index equals two
	Time Tag	020C (H)
	Data Word #1	020E (H)
	Data Word #2	0210(H) Index decrements to one
Command #3 Receive three words	Message Info Word	0212 (H) Index equals one
	Time Tag	0214 (H)
	Data Word #1	0216 (H)
	Data Word #2	0218(H)
	Data Word #3	021A (H) Index decrements to zero
		[Data pointer A updated to 010e (H), interrupt generated enabled]

Figure 4-3 RT Non-broadcast Receive Message Indexing

X = don't care

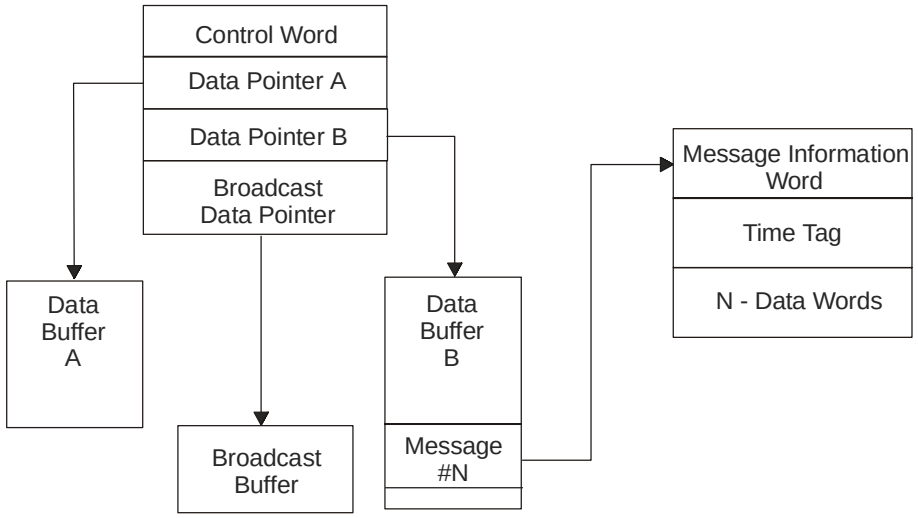

Figure 4-4 *M8K1553MCH* Descriptor Block – Receive

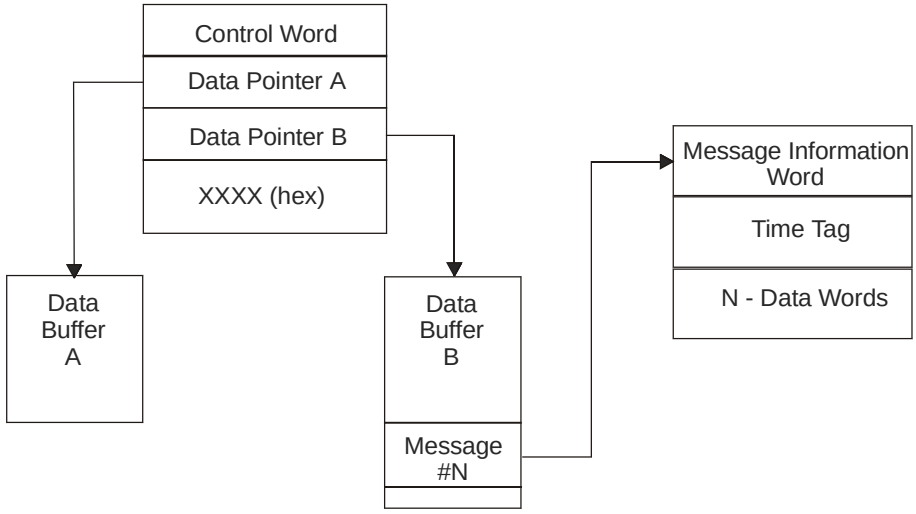

Figure 4-5 *M8K1553MCH* Descriptor Bock – Transmit

4.2.6 Ping-pong Handshake (Mode #0)

The *M8K1553MCH* provides a mechanism to enable and disable buffer ping-pong operation. If ping-pong is enabled during Remote Terminal operation, data will be stored/retrieved in alternative buffers each time a new message is processed. If ping-pong is disabled a single buffer will be used for all message processing.

The Handshake mechanism operates as follows:

Prior to starting Remote Terminal operation, enable the buffer ping-pong feature by writing a logical 1 to bit 02 of the Control Register. During ping-pong operation, the remote terminal ping-pongs between the two data buffers, for each subaddress or mode code, on a message-by-message basis. Each unique MIL-STD-1553 subaddress and mode code is assigned two data buffer locations (A and B). The remote terminal retrieves data from a buffer or stores data into a buffer depending on the message type (i.e., transmit or receive Command). During ping-pong operation, the Remote Terminal determines the active subaddress or mode code buffer at the beginning of message processing, the remote terminal complements bit 02 of the Descriptor Control Word to access the alternate buffer on the following message (i.e., ping-pong).

The application software disables ping-pong operation by writing a logical 0 to Control Register bit 02. The disable of ping-pong operation is acknowledged by bit 09 of the Control Register. Bit 09 of the Control Register acknowledges the ping-pong disable by transitioning from a logical 1 to a logical 0. The application software interrogates bit 02 of each Descriptor Control Word to determine the active buffer on a subaddress or mode code basis. If bit 02 is a logical 0, the remote terminal uses Buffer A and the application software off-loads or loads Buffer A.

The application software enables ping-pong operation by writing a logical 1 to Control Register bit 02. The enable of ping-pong operation is acknowledged by bit 09 of the Control Register. Bit 09 of the Control Register acknowledges the ping-pong enable by transitioning from a logical 0 to a logical 1.

4.2.7 Broadcast Data Pointer (Mode #0)

The Broadcast Data Pointer contains the address for the Message Information Word, Time Tag Word, and Data Words associated with a broadcast Command. The following bits describe the receive subaddress/mode code descriptor Broadcast Data Pointer. If ping-pong operation is disabled, the module automatically increments this Data

Pointer during Command post-processing,

Bit	Bit Name	Description
00-15	**BP[15-0]**	Broadcast Data Pointer. The fourth Word of the descriptor block contains the broadcast data buffer location. This pointer can reside anywhere in memory space. The module accesses this pointer when Control Word bit 00 is a logic 1 and broadcast is enabled. Bit 15 is the most significant bit, bit 00 is the least significant bit. **Note** 1. If ping-pong is enabled, this pointer does not update. 2. When the broadcast Command is followed by a Transmit Last Command or Last Status Word mode code, the module transmits a Status Word with bit 15 of the Status Word set to a logic 1. The broadcast bit is cleared when the next valid non-Broadcast Command is received.

Broadcast Data Pointer

4.3 Data Structures

The following sections discuss the Data structures that result from Command processing. For each complete message processed, the *M8K1553MCH* generates a Message Information Word and Time Tag Word. These Words aid the host in further message processing. The Message Information Word contains Word count, message type, and message error information. The Time Tag Word is a 16-bit Word containing the Command validity time. The Time Tag Word data comes from the module's internal Time Tag counter.

4.3.1 Subaddress Receive Data

For receive Commands, the module stores Data Words plus two additional Words. The module adds a Receive Information Word and Time Tag Word to each receive Command data packet. The module places the Receive Information Word and Time Tag Word ahead of the Data Words associated with a receive Command (see Figures 4-3, 4-4 and4-5 above). When message errors occur, the module stores the Receive Information Word and Time Tag Word. Once a message error condition is observed, all Data Words are considered invalid.

Data storage occurs at the memory location pointed to by the Data pointer plus two 16-bit locations.

RECEIVE INFORMATION WORD

The Receive Information Word contents are:

Bit	Bit Name	Description
11-15	**WC[4-0]**	Word Count Bits. These five bits contain Word count information extracted from the Command Word bits 15 to 19.
10	**Reserved**	Ignore on read.
09	**BUA/B**	Bus A/B. 1 = The message was received on Bus A. 0 = The message was received on Bus B.
08	**RTRT**	Remote Terminal to Remote Terminal Transfer. The Command processed was an RT-to-RT transfer.
07	**ME**	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	**Reserved**	Ignore on read.
04	**ILL**	Illegal Command Received. 1 = The Command received was an illegal Command.
03	**TO**	Time-Out Error. 1 = The module did not receive the proper number of Data Words, i.e., the number of Data Words received was less than the Word count specified in the Command Word.
02	**OVR**	Overrun Error. 1 = The module received a Word when none was expected or the number of Data Words received was greater then expected.
01	**PRTY**	Parity Error. 1 = The module observed a parity error in the incoming Data Words.
00	**MAN**	Manchester Error. 1 = The module observed a Manchester error in the incoming Data Words.

Receive Information Word

4.3.2 Subbaddress Transmit Data

The user is responsible for organizing the data packet (i.e., *N* Data Words) into memory and establishing the applicable Data Pointer. The user can allocate two 16-bit memory locations at the top of the data packet for the storage of the Transmit Information Word and the Time Tag Word. An example transmit Data structure for three Words is shown below:

Data Pointer A —→	0200 (H)	XXXX	Reserved for Transmit Info Word
equals 0100 (H)	0202 (H)	XXXX	Reserved for Time Tag Word
	0204 (H)	FFFF	Data Word #1
	0206 (H)	FFFF	Data Word #2
	0208 (H)	FFFF	Data Word #3

Note Data pointer A points to the top of the Data structure, not to the top of the Data Words.

TRANSMIT INFORMATION WORD

The Transmit Information Word contents are:

Bit	Bit Name	Description
11-15	**WC[4-0]**	Word Count Bits. These five bits contain Word count information extracted from the Command Word bits 15 to 19.
10	**Reserved**	Ignore on read.
09	**BUA/B**	Bus A/B. 1 = The message was received on Bus A. 0 = The message was received on Bus B.
08	**Reserved**	Ignore on read.
07	**ME**	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for more detail.
05-06	**Reserved**	Ignore on read.
04	**ILL**	Illegal Command Received. 1 = The Command received was an illegal Command.
03	**Reserved**	Ignore on read.
02	**OVR**	Overrun Error. 1 = The module received a Data Word with a Transmit Command.
00-01	**Reserved**	Ignore on read.

Transmit Information Word

4.3.3 Mode Code Data

The Transmit and Receive Data Structures for mode codes are similar to those for a subaddress. The receive Data structure contains an Information Word, Time Tag Word, and message Data Word. All receive mode codes with data have one associated Data Word. Data storage occurs at the memory location pointed to by the Data pointer plus two 16-bit locations. Reception of the synchronize with Data mode code automatically loads the Time Tag counter and stores the Data Word at the address defined by the Data pointer plus two 16-bit locations.

The transmit mode code Data structure contains an Information Word, Time Tag Word, and associated Data Word. The host is responsible for linking the module Data Pointer to the data (e.g., Transmit Vector Word). For mode codes with internally generated Data Words (e.g., Transmit BIT Word, Transmit Last Command), the transmitted Data Word is added to the Data structure.

For MIL-STD-1553A mode of operation, all mode codes are defined without Data Words. For mode codes without data, the Data structure contains the Message Information Word and Time-Tag Word only.

Note In MIL-STD-1553A all mode codes are without data and the T/R bit is ignored.

MODE CODE RECEIVE INFORMATION WORD

The Mode Code Receive Information Word contents:

Bit	Bit Name	Description
11-15	**MC[4-0]**	Mode Code. These five bits contain the mode code information extracted from the receive Command Word bits 15 to 19.
10	**Reserved**	Ignore on read.
09	**BUA/B**	Bus A/B. 1 = The message was received on Bus A. 0 = The message was received on Bus B.
08	**RTRT**	Remote Terminal to Remote Terminal Transfer. 1 = The Command processed was an RT-to-RT transfer.
07	**ME**	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	**Reserved**	Ignore on read.
04	**ILL**	Illegal Command Received. 1 = The Command received was an illegal Command.
03	**TO**	Time-out Error. 1 = The module did not receive the proper number of Data Words, i.e., the number of Data Words received was less than the Word count specified in the Command Word.
02	**OVR**	Overrun Error. 1 = The module received a Word when none was expected, or the number of Data Words received was greater than expected.
01	**PRTY**	Parity Error. 1 = The module observed a parity error in the incoming Data Words.
00	**MAN**	Manchester Error. 1 = The module observed a Manchester error in the incoming Data Words.

Mode Code Receive Information Word

MODE CODE TRANSMIT INFORMATION WORD

The Mode Code Transmit Information Word contents are:

Bit	Bit Name	Description
11-15	**MC[4-0]**	Mode Code. These five bits contain the mode code information extracted from the Command Word bits 15 to 19.
10	**Reserved**	Ignore on read.
09	**BUA/B**	Bus A/B. 1 = The message was received on Bus A. 0 = The message was received on Bus B.
08	**Reserved**	Ignore on read.
07	**ME**	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	**Reserved**	Ignore on read.
04	**ILL**	Illegal Command Received. 1 = The Command received was an illegal Command.
03	**Reserved**	Ignore on read.
02	**OVR**	Overrun Error. 1 = The module received a Data Word with a Transmit Command.
00-01	**Reserved**	Ignore on read.

Mode Code Transmit Information Word

4.4 RT Circular Buffer Modes

The RT circular buffer modes simplify the software service of remote terminals implementing bulk or periodic data transfers. Select the preferred mode at start-up by writing to Control Register bits 07 and 08 (see **Control Register** on page 4-3). The two modes, Mode #1 and Mode #2 are discussed in sections 4.4.1 and 4.4.2

4.4.1 Mode #1 Operation

In this mode the module merges transmit or receive data into a circular buffer along with message information.

For each valid receive message, the module enters a message information Word, Time-Tag Word, and Data Word(s) into a unique receive circular buffer.

For each valid transmit message, the module enters a message information Word and Time Tag Word into reserved memory locations within the transmit circular buffer. The module automatically controls the wrap around of circular buffers.

4.4.1.1 MODE #1 DESCRIPTOR BLOCK

Each subaddress and mode code both transmit and receive, has a unique circular buffer assignment. The module decodes the Command Word T/R bit, subaddress/mode code field, and Word_count/mode_code field to select a unique descriptor block that contains Control Word, TA, CA, and BA (see Figure 4-6).

To implement Circular Buffer 1's architecture, the 4-word descriptor block and Control Register are different than in the Mode #0. Bits 15 through 08 of the Control Word are 'don't care'. The second Word of the descriptor block defines the buffer's starting or top address (TA). The TA pointer remains static during message processing. The fourth entry into the descriptor block identifies the buffer's bottom address (i.e., BA) and remains static during message processing. The third descriptor block Words represent the current address (i.e., CA) in the buffer and is dynamic. If the module observes no message error conditions, the CA pointer updates at the end of message processing. The application software reads the dynamic CA pointer to determine the current bottom of the buffer.

The TA (top of buffer) and BA (bottom of buffer) pointers define the circular buffer's length. The CA pointer identifies the current address (i.e., last accessed address plus one). The circular buffer wraps to the top address after completing a message that results in CA being greater than or equal to BA. If CA increments past BA during intra-message processing, the module will access memory (read or write) address locations past BA. Delimit all circular buffer boundaries with at least 34 address locations.

Note In this mode of operation, bits INDX, NII and A/B of the descriptor Control Word and the PPEN bit of the Control Register are 'don't care'.

4.4.1.2 MODE #1 CIRCULAR BUFFER — RECEIVE MESSAGE PROCESSING

The module begins all message processing by reading a unique descriptor block after reception and validation of a subaddress or mode code Command Word. The module internally increments the CA pointer to store the receive Data Word(s). After message processing completes, the module stores the Message Information Word and Time-Tag Word into the circular buffer preceding the message data. At the end of message processing, the module updates CA (if no errors detected). For CA larger than BA storage of next message begins at the address location pointed to by the TA pointer, and CA is made equal to TA. If CA is less than BA, CA points to the next available memory location in the buffer (i.e., CA+1).

For transmit Commands, the module begins transmission of data from memory location CA+2. Reserve the first two locations for the message information Word and Time Tag Word. After message processing completes, the module enters the message information Word and Time Tag Word into the circular buffer. At the end of message processing, the module updates CA (if no errors detected). For CA larger than BA, storage of the next message begins at the address location pointed to by the TA pointer, and CA is made to equal TA. If CA is less than BA, CA points to the next available memory location in the buffer (i.e., CA+1).

Note In this mode the Message Information Word bit 5 reflects the reception of broadcast message via the BRD bit.

The module generates a circular buffer empty/full interrupt when the buffer reaches the end (i.e., CA greater than BA) and begins a new message at the top of the buffer. Bit 08 of the Mask Register and bit 07 of the Descriptor Control Word mask enables the generation of the Full/Empty interrupt.

Figure 4-6 describes the relationship between the top address (TA), bottom address (BA) and current address (CA):

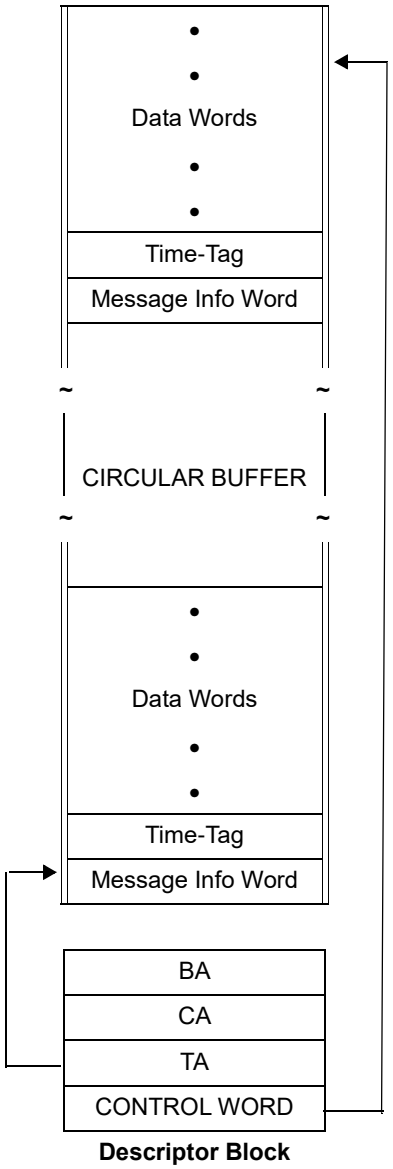

Figure 4-6 RT Mode #1 Descriptor Block And Circular Buffer

4.4.2 Mode #2 Operation

In this mode, the module separates message data and message information into unique circular buffers. The separation of data from message information simplifies the software that loads and unloads data from the buffers. The message information buffer contains Time-Tag and Message Information Words for each message transacted on the bus, while the data buffer contains the message Data Words. After processing a pre-determined number of messages, both buffers wrap-around.

4.4.2.1 MODE #2 DESCRIPTOR BLOCK

Each subaddress and mode code, both transmit and receive, has a unique pair of circular buffers. The module decodes the Command Word T/R bit, subaddress/ mode field, and Word_count/mode_code field to select a unique descriptor block that contains Control Word, TA, CA, and MIB (see Figure 4-7 on page 4-34).

To implement Circular Buffer 2's architecture, the descriptor block and Control Register are different than in Mode #0. Bits 15 through 08 of the Control Word specify the Message Information Buffer (MIB) length; the maximum MIB size is 256. Table 4-3 shows how the Control Word's most significant bits select the depth of the MIB. The Control Words eight most significant bits remain static during message processing.

The second Word of the description block defines the top address (TA) of the Data circular buffer. The TA pointer remains static during message processing. The third descriptor Word identifies the current address (i.e., CA) of the Data circular buffer. The application software reads the dynamic CA pointer to determine the current address of the Data buffer. The module increments the CA pointer, at the end of message processing, until the MIB buffer is full. When the MIB wraps around, the SμMMIT loads the CA pointer with the TA pointer.

The fourth Word in the descriptor block defines the top or base address of the Message Information Buffer (i.e., MIB) and the current MIB address (i.e., offset from base address). The SμMMIT enters the message information Word and Time-Tag Word into the MIB, for each message, until the end of the MIB is reached. When the MIB reaches the end, the next message's message information Word and Time-Tag Word is entered at the top of the MIB. The MIB pointer is a semi-static pointer. The module updates the current address field at the end of message processing. The Base Address field remains static.

Note In this mode of operation, bits INDX, NII and A/B of the descriptor Control Word and the PPEN bit of the Control Register are 'don't care'.

4.4.2.2 MODE #2 CIRCULAR BUFFER — RECEIVE MESSAGE PROCESSING

The module begins all message processing by reading the descriptor block of the subaddress or mode code Command received (i.e., Control Word, TA, CA, and MIB). The module begins storage of Data Word(s) starting at the location contained in the CA pointer. The module automatically updates the CA pointer internally as message processing progresses. The module stores the message information Word and Time-Tag Word into the MIB, after receiving the correct number of Data Words, At the end of message processing, the module updates CA and the MIB Current Address Field (CAF). If CAF equals the specified MIB length, CA is updated to TA and the MIB CAF is reset to zero. If CAF is less than the specified MIB length, CA and MIB CAF point to the next available memory location in each buffer. Control Word bits 15 to 08 specify the MIB length.

For transmit Commands, the module begins transmission of data from memory location CA. After message processing completes, the module enters the message information Word and Time Tag Word into the MIB. At the end of message processing, the module updates CA and the MIB CAF. If CAF equals the specified MIB length, CA is updated to TA and the MIB CAF is reset to zero. If CAF is less than the specified MIB length, CA and MIB CAF point to the next available memory location in each buffer.

Note In this mode the BRD bit is added to the Message Information Word bit 05.

The module generates a circular buffer empty/full interrupt when the MIB reaches the end and begins a new message at the top of the buffer. Bit 08 of the Mask Register and bit 07 of the Descriptor Control Word mask enable the generation of the Full/Empty interrupt.

Control Word Bits 8-15	Length of MIB (messages)	MIB Pointer Structure (Base and CAF)
FF	128	8 Bit Base Address +8 Bit Current Address Field
7F	64	9 Bit Base Address +7 Bit Current Address Field
3F	32	10 Bit Base Address +6 Bit Current Address Field
1F	16	11 Bit Base Address +5 Bit Current Address Field
0F	8	12 Bit Base Address +4 Bit Current Address Field
07	4	13 Bit Base Address +3 Bit Current Address Field
03	2	14 Bit Base Address +2 Bit Current Address Field
01	1	15 Bit Base Address +1 Bit Current Address Field

Table 4-3: RT Mode #2 Control Word and MIB Pointer Structure

Figure 4-7 describes the relationship between the top address (TA), current address (CA) and Message Information Buffer (MIB):

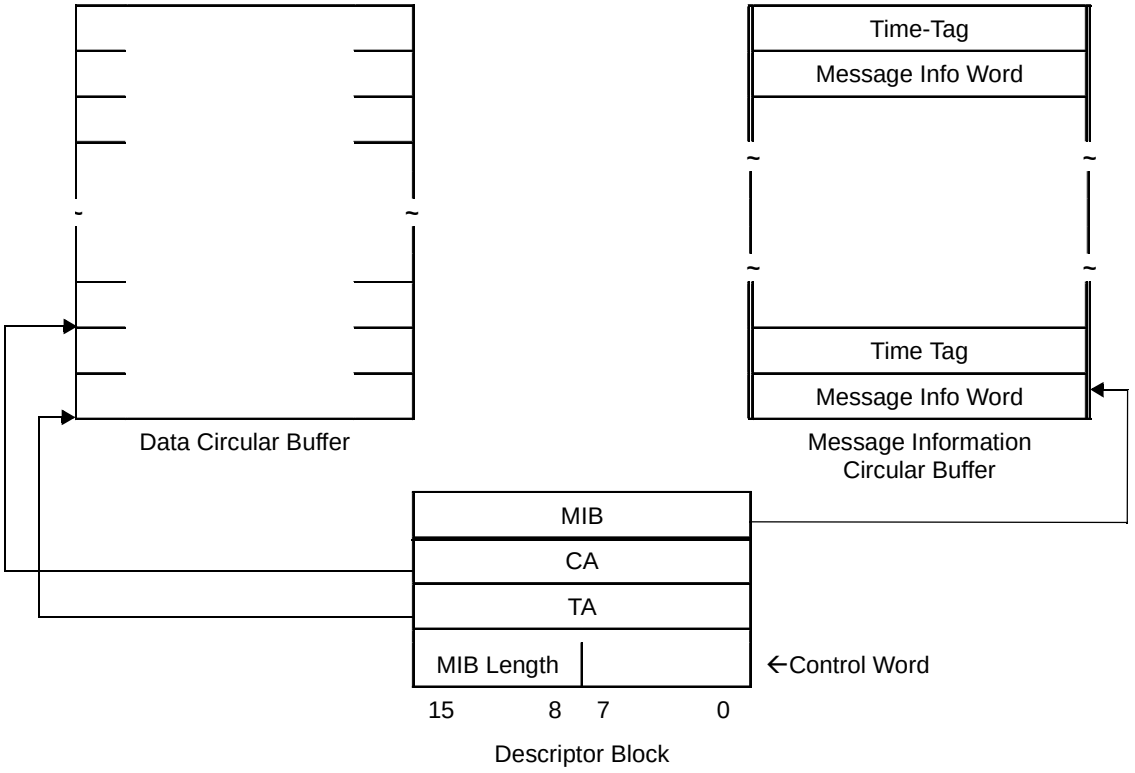

Figure 4-7 RT Mode #2 Descriptor Block

4.5 Mode Code And Subaddress

The *M8K1553MCH* provides subaddress and mode code decoding that meets MIL-STD-1553B requirements. In addition, the module has automatic internal illegal Command decoding for reserved. MIL-STD-1553B mode codes. Table 4-4 shows the module's response to all possible mode code combinations.

Table 4-4: Mode Code Descriptions

T/R	Mode Code (Hex)	Mode Code (Dec)	Function	Operation
0	00000 – 01111	0 – 15	Undefined (w/o data)	1. Command Word stored 2. Status Word transmitted
0	10000	16	Undefined (with data)	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10001	17	Synchronize (with data)	1. Command Word stored 2. Data Word stored 3. Time-Tag counter loaded with Data Word value 4. Status Word transmitted
0	10010	18	Undefined	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10011	19	Undefined	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10100	20	Selected Transmitter Shutdown	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10101	21	Override Selected Transmitted Shutdown	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10110 – 11111	22 – 31	Reserved	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
1	00000	0	Dynamic Bus Control	1. Command Word stored 2. Dynamic Bus Acceptance bit set in outgoing Status Word if enabled in the Control Register 3. Status Word transmitted
1	00001	1	Synchronize	1. Command Word stored 2. Time Tag counter reset to 0000 (H) 3. Status Word transmitted

Table 4-4: Mode Code Descriptions (Continued)

T/R	Mode Code (Hex)	Mode Code (Dec)	Function	Operation
1	00010	2	Transmit Status Word	1. Command Word stored 2. Last Status Word transmitted 3. Status Word cleared after reset **Note**: The module updates Status Word if illegalized.
1	00011	3	Initiate Self-Test	1. Command Word stored 2. Status Word transmitted 3. BIT initiated 4. TF bit set if BITF bit asserted
1	00100	4	Transmitter Shutdown	1. Command Word stored 2. Status Word transmitted 3. Alternate bus disabled
1	00101	5	Override Transmitter Shutdown	1. Command Word stored 2. Status Word transmitted 3. Alternate bus enabled **Note**: Reception of the override transmitter shut-down mode code does not enable a module not previously enabled in the Control Register. Reset remote terminal mode code clears the transmitter shutdown function.
1	00110	6	Inhibit Terminal Flag Bit	1. Command Word stored 2. Terminal flag bit set to 0 and assertion disabled 3. Status Word transmitted
1	00111	7	Override Inhibit Terminal Flag	1. Command Word stored 2. Terminal flag bit enabled for assertion 3. Status Word transmitted
1	01000	8	Reset Remote Terminal	1. Command Word stored 2. Status Word transmitted 3. Software reset
1	01001 – 01111	9 – 15	Reserved	1. Command Word stored 2. Status Word transmitted
1	10000	16	Transmit Vector Word	1. Command Word stored 2. Service request bit set to a logic zero in out going Status 3. Status Word transmitted 4. Data Word transmitted 5. Clears the SRQ bit in the 1553 Status Word Bits Register
1	10001	17	Reserved	1. Command Word stored 2. Status Word transmitted 3. Data Word stored

Table 4-4: Mode Code Descriptions (Continued)

T/R	Mode Code (Hex)	Mode Code (Dec)	Function	Operation
1	10010	18	Transmit Last Command	1. Command Word stored 2. Last Status Word transmitted 3. Last Command Word transmitted 4. Data Word stored (Transmit Last Command 5. Transmitted Data Word is all 0 after reset **Note**: The module stores the Transmit Last Command mode code if illegalized and updates Status Word.
1	10011	19	Transmit BIT Word	1. Command Word stored 2. Status Word transmitted 3. BIT Word transmitted from BIT Word Register 4. Data Word stored (Transmit BIT Word)
1	10100 – 10101	20 – 21	Undefined (with data)	1. Command Word stored 2. Status Word transmitted 3. Data Word transmitted
1	10110 – 11111	22 – 31	Reserved	1. Command Word stored 2. Status Word transmitted 3. Data Word transmitted

4.6 Encoder and Decoder

The *M8K1553MCH* receives the Command Word from the MIL-STD-1553 bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the Command is a receive Command, the module processes each incoming Data Word for correct format, Word count, and contiguous data. If a message error is detected, the module stops processing the remainder (if any) of the message, suppresses Status Word transmission, and asserts bit 09 (ME bit) of the Status Word.

The module automatically compares the transmitted Word (encoder Word) with the reflected decoder Word by way of the continuous loopback feature. If the encoder Word and reflected Word do not match, the WRAPF bit is asserted in the BIT Word Register and an interrupt will be generated, if enabled. In addition to the loopback compare test, a timer precludes a transmission greater than 800ìsec. by the assertion of Fail-Safe Timer. This timer is reset upon receipt of another Command.

Remote Terminal Response-Time:

MIL-STD-1553A = 7 µsec.
MIL-STD-1553B = 10 µsec.
Data Contiguity Time-Out = 1.0 msec.

4.7 RT-to-RT Transfer Compare

The RT-to-RT Terminal Address compare logic ensures that the incoming Status Word's Terminal Address matches the Terminal Address of the transmitting RT specified in the Command Word. An incorrect match results in setting the message-error bit and suppressing transmission of the Status Word. (RT-to-RT transfer time-out = 55 to 59 µsec.). The module does not check ME or SSYSF of the transmitting remote terminal when receiving.

4.8 Terminal Address

The *M8K1553MCH* Terminal Address is programmed via the most significant six bits in the Operational Status Register: RTA[4-0] and RTPTY. The Terminal Address parity is odd; RTPTY is set to a logic state to satisfy this requirement. When the Operational Status Register bit 02 (TAPF) is set, this indicates incorrect Terminal Address parity. The Operational Status Register bit 02 is valid after the rising (final) edge of a reset.

For example:

RTA[4-0] = 05(H) = 00101
RTPTY = 1(H) = 1 Sum of 1s = 3 (odd), Operational Status Register Bit 02 = 0
RTA[4-0] = 04 (H) = 00100
RTPTY = 0 (H) = 0 Sum of 1s = 1 (odd), Operational Status Register Bit 02 = 0
RTA[4-0] = 04 (H) = 00100
RTPTY = 1 (H) = 0 Sum of 1s = 2 (even), Operational Status Register Bit 02 = 0

Note The module checks the Terminal Address and parity after RT mode operation has been started. With Broadcast disabled, RTA(4:0) = 11111 operates as a normal RT address.

The BIT Word Register parity fail bit is valid after RT mode has been started.

The Terminal Address is also programmed via a write to the Operational Status Register. The module loads the Terminal Address upon completion of the Control Register write that activates RT mode.

4.9 Reset

The software reset (see **Module Reset Register** on page 2-2) is also equivalent to a hardware (power-on) reset and takes 5 µsec. to complete. Setting the Reset bit to 1 results in the immediate reset of the module and termination of Command processing. The user is responsible for the re-initialization of the RT Mode for operation.

A Reset Remote Terminal mode code (Mode Code 01000, T/R = 1) clears the encoder/decoders, resets the Time Tag, enables the buses to the programmed host state, and re-enables the Terminal Flag for assertion. This reset is performed after the transmission of the 1553 Status Word.

4.10 MIL-STD-1553A/B Operation: RT Mode

To maximize flexibility, the *M8K1553MCH* can operate in many different systems that use various protocols. Specifically, two of the protocols that the module may be used with are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, configure the module through the Control register (XMTSW Bit 00) and the Operational Status register (A/B_STD Bit 07).

Table 4-5 defines the three ways to program the module.

A/B STD	XMTSW	RESULT (protocol selected)
0	X	1553B response, 1553B Standard
1	0	1553A response, 1553A Standard
1	1	1553A response, auto execute the TRANSMIT STATUS WORD mode code.

Table 4-5: MIL-STD-1553A/B Operation: RT Mode

When configured as a remote terminal to meet MIL-STD-1553A, the *M8K1553MCH* will operate as follows:

- Responds with a Status Word within 7µsec.
- Ignores the T/R bit for all mode codes.
- All mode codes are defined without data.
- All mode codes use mode code transmit control and information Words.
- Mode code 00000 is defined as dynamic bus control (DBC).
- Subaddress 00000 defines a mode code.
- ME and TF bits are defined in the 1553 Status Word; all other Status Word bits are programmable (i.e., NO BUSY mode, etc.)
- Broadcast of all mode codes, except Mode Code 00000 (DBC) and mode code 00010 (transmit Status Word if enabled), is allowed.
- To illegalize a Mode Code, the user needs to illegalize both the receive and transmit versions.
- Illegalization of row 1F (H) is not automatic.

5 Bus Monitor Operation

Chapter 5 describes *M8K1553MCH* operation in Bus Monitor (BM) mode. The topics covered are:

5.1 Bus Monitor Message Processing

To process messages, the *M8K1553MCH* uses data supplied in the Control Registers along with RAM memory. There are eight 16-bit memory locations for each message called a monitor block, seven are used and one is reserved. The monitor block is updated at the end of command processing. The following paragraphs discuss the command block in detail.

The user allocates memory spaces for each monitor block. The top of the monitor blocks can reside at any address location. The Control Registers are initialized by the host and linked to the Monitor Block via the Initial Monitor Block Pointer Register and the Monitor Block Counter Register contents. Each monitor block contains a Message Information Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, and Time Tag. For a full description of each location, see section **5.3 Bus Monitor Architecture** on page 5-11.

The Message Information Word allows the module to inform the user on which bus the command was received, whether the message was an RT-to-RT transfer, and conditions associated with the message. The module also stores each Command Word associated with the message in the appropriate location. For normal 1553 commands, only the first Command Word location will contain data. For RT-to-RT commands, the second Command Word location will contain data, and bit 08 in the Message Information Word will be set.

For each command, the Data Pointer is read to determine where to store data words. The module stores data sequentially from the top memory location. The module also stores each status word associated with the message in the appropriate location. For normal 1553 commands, only the first status word location will contain data. For RT-to-RT commands, the second status word location will contain data.

The module begins monitoring after Control Register bit 15 = 1 (i.e., Setting TERACT and STEX bits to 1). After reception, the module begins post-processing. Command post-processing involves storing data to memory. An optional interrupt log entry is performed after a monitor is entered. Monitor Time-Out:

- MIL-STD-1553A = 9 µsec.
- MIL-STD-1553B = 15 µsec.

5.1.1 Error Condition Message Processing

When the monitor detects as error condition, either, in the Command Word, Data Words, or the RT's status, the monitor block will not store the data. The monitor block counter increments. The initial message Data Pointer remains constant. The monitor block pointer increments. Message information bits of the monitor block are changed to reflect the error. An interrupt is given indicating a message has occurred.

See Message Information Bits, page 5-11.

5.2 Control Registers: BM Mode

The control registers are read/write unless otherwise stated. All control registers **must** be accessed in word mode. All Control Register bits are active high and are reset to 0 unless otherwise stated.

Figure 5-1 illustrates the control registers for Bus Monitor mode.

Reserved	0020-003E H
Monitor Filter Register Lo	001E H
Monitor Filter Register Hi	001C H
Monitor Block Counter Register	001A H
Initial Monitor Data Pointer Register	0018 H
Initial Monitor Command Block Pointer Register	0016 H
Reserved	0010-0014 H
Time Tag Register	000E H
BIT Word Register	000C H
Interrupt Log List Pointer Register	000A H
Pending Interrupt Register	0008 H
Interrupt Mask Register	0006 H
Current Command Block Register	0004 H
Operational Status Register	0002 H
Control Register	0000 H

Figure 5-1 Control Registers Map: BM Mode

5.2.1 Control Register

Address: 0000 (H)
Read/Write

Use the Control Register to configure the module for BM operation. To make changes to the BM and to this register, the STEX bit (bit 15) must be logic 0.

Note The user has 5 µsec. after the TERACT bit (bit 00 of the Operational Status Register) is active, to stop operation.

Bit	Bit Name	Description
15	**STEX**	Start Execution 1 = Initiates module operation 0 = Inhibits module operation After execution begins, writing a logic 0 will halt the module after completing the current 1553 message.
14	**SBIT**	Start BIT 1 = Places the module into the Built-In Test routine. The BIT test takes 1 msec. to execute and has a fault coverage of 93.4%. Once the module has been started, the host must halt the module in order to place it into the Built-In Test mode (STEX = 0). **Note** If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
11-13	**Reserved**	Set to 0
10	**ETCE**	External Timer Clock Enable 1 = Enables an external clock used with an internal counter for variable minor frame timing **Note** The user can only change the clock frequency before starting the device (i.e. setting bit 15 of register 0 to a login 1.
09	**ERTO**	Extended Response Time-Out 1 = Enables the extended response time-out option and forces the BM Mode to look for an RTs response time in 30 µsec. or generate time-out errors. 0 = Enables for the standard time-out in 14 µsec.
06-08	**Reserved**	Set to 0
05	**BMTC**	Bus Monitor Control. This bit determines whether the module will monitor all RTs or selected RTs. 1 = The module will monitor only the RTs as specified in the Monitor Filter Hi and Lo registers. 0 = The module will monitor all RTs.
04	**BCEN**	Broadcast Enable 1 = Enables RT #31 to be used as a message broadcast 0 = Enables RT #31 as a normal address.
02-03	**Reserved**	Set to 0
01	**INTEN**	Interrupt Log List Enable. 1 = Enables the interrupt log list. 0 = Prevents the logging of interrupts as they occur.
00	**Reserved**	Set to 0

Control Register

5.2.2 Operational Status Register

Address: 0002 (H)
Read/Write

The Operational Status Register reflects pertinent status information for the module and is not reset to 0000 (H) on reset. Instead, the bit A/B_STD is set to 1.

Note To make changes to the Monitor and this register, the STEX bit (Bit 15 in the Control Register) must be logic 0.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**MSEL1**	Mode Select 1. In conjunction with Mode Select 0, this bit determines the module's mode of operation.
08	**MSEL0**	Mode Select 0. In conjunction with Mode Select 1, this bit determines the module's mode of operation.

MSEL1	MSEL0	Mode of Operation
0	0	BC
0	1	RT
1	0	BM
1	1	RT/ Concurrent BM Mode

07	**A/B_STD**	Military Standard 1553A or 1553B. This bit determines if the module will operate under MIL-STD-1553A or 1553B protocol. 1 = Forces the module to declare a time-out error condition if the RT9 has not responded in 9 μsec. 0 = Allows the module to declare a time-out error condition if the RT has not responded in 15 μsec.
04-06	**Reserved**	These read-only bits are not applicable.
03	**EX**	Module Executing. This read-only bit indicates whether the module is presently executing or is idle. 1 = The module is executing. 0 = The module is idle.
02	**Reserved**	This read-only bit is not applicable.
01	**Ready**	Module-Ready. This read-only bit is cleared on reset. 1 = The module has completed initialization or BIT, and regular operation may begin.
00	**TERACT**	module Terminal Active. This read-only bit is cleared on reset. 1 = The module is presently processing a 1553 message. **Note** When STEX transitions from 1 to 0, EX and TERACT stay active until command processing is complete.

Operational Status Register

5.2.3 Current Command Register

Address: 0004 (H)
Read only

The Current Command register contains the last valid command that was transmitted over the 1553 bus. In an RT-to-RT transfer, this register will update as each of the two commands are received by the Bus Monitor.

Bit	Bit Name	Description
00-15	**CC[15-0]**	Current Command. These bits contain the latest 1553 command that was transmitted by the Bus Monitor.

Current Command Register

5.2.4 Interrupt Mask Register

Address: 0006 (H)
Read/Write

The *M8K1553MCH* interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked only if the corresponding bit of this register is set to a logic 0.

Bit	Bit Name	Description
12-15	**Reserved**	Set to 0
11	**MERR**	Message Error Interrupt
01-10	**Reserved**	Set to 0
00	**MBC**	Monitor Block Counter Interrupt

Interrupt Mask Register

5.2.5 Pending Interrupt Register

Address: 0008 (H)
Read only

The Pending Interrupt register is used to identify which of the interrupts occurred during operation. All register bits are cleared on a host read.

Bit	Bit Name	Description
12-15	**Reserved**	Ignore on read.
11	**MERR**	Message Error Interrupt 1 = A message error occurred. The module can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated (if not masked) after message processing is complete.
01-10	**Reserved**	Ignore on read.
00	**MBC**	Monitor Block Counter Interrupt This bit is set if the module's monitor block counter reaches 0 (transition from 1 to 0) **Note** The monitor does not discriminate between error-free messages and those messages with errors

Pending Interrupt Register

5.2.6 Interrupt Log List Pointer Register

Address: 000A (H)
Read/Write

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts.

The *M8K1553MCH* architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K-word memory space. Initialize the lower 5 bits of this register to a logic 0 by the host. The module controls the lower 5 bits to implement the ring-buffer architecture. Read this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Bit	Bit Name	Description
00-15	**ILLP[15-0]**	Interrupt Log List Pointer Bits. **Note** Bits 05-15 indicate the starting Base address while bits 00-04 indicate the ring location of the Interrupt Log List.

Interrupt Log List Pointer Register

5.2.7 BIT Word Register

Address: 000C (H)
Read/Write

The BIT Word register contains information on the current status of the module hardware. The user defines the lower 8 bits of this register.

Bit	Bit Name	Description
15	**DMAF**	DMA Fail. 1 = All the module's internal DMA activity was not completed within 7 µsec.
13-14	**Reserved**	Ignore on read
12	**BITF**	BIT Fail. 1 = A BIT failure. Interrogate bits 11and 10 to determine the specific bus that failed.
11	**BUAF**	Bus A Fail. 1 = A BIT test failure in Bus A.
10	**BUBF**	Bus B Fail. 1 = A BIT test failure in Bus B.
09	**MSBF**	Memory Test Fail. Most significant memory byte failure.
08	**LSBF**	Memory Test Fail. Least significant memory byte failure.
00-07	**UDB[7-0]**	User-Defined Bits.

BIT Word Register

5.2.8 Time Tag Register

Address: 000E (H)
Read only

The Time Tag register reflects the state of a 16-bit free running ring counter in the RT and Bus Monitor modes. This counter will remain a free running counter as long as the module is not in a reset mode. The resolution of this counter is 64 µsec/bit. The Time Tag counter begins operation on the falling (final) edge of the reset pulse.

Bit	Bit Name	Description
00-15	**TT[15-0]**	Time Tag Counter Bits. These bits indicate the state of the 16-bit internal counter.

Time Tag Register

5.2.9 Initial Monitor Block Pointer Register

Address: 0016 (H)
Read/Write

The Initial Monitor Block Pointer register contains the starting location of the Monitor Blocks.

Note Do not change this register while BM mode is active (i.e., Operational Status Register, bit 03 = 1).

Bit	Bit Name	Description
00-15	MBA[15-0]	Initial Monitor Block Address. These bits indicate the starting location of the Monitor Block.

Initial Monitor Block Pointer Register

5.2.10 Initial Monitor Data Pointer Register

Address: 0018 (H)
Read/Write

The Initial Monitor Data Pointer register contains the starting location of the Monitor Data.

Note Do not change this register while BM mode is active (i.e., Operational Status Register, bit 03 = 1).

Bit	Bit Name	Description
00-15	MBA[15-0]	Initial Monitor Data Address. These bits indicate the starting location of the Monitor Data.

Initial Monitor Data Pointer Register

5.2.11 Monitor Block Counter Register

Address: 001A (H)
Read/Write

The Monitor Block Counter register contains the number of Monitor Blocks the user wants to log. After execution begins, the register automatically decrements as commands are logged. When the register is decremented from 1 to 0, an interrupt will be generated, if enabled. The module will start over at the initial pointers as identified in the Initial Monitor Block Pointer Register and the Initial Monitor Data Pointer Register.

Note It is recommended that this register not be changed while the BM mode is active (i.e., Operational Status Register, bit 03 = 1).

Bit	Bit Name	Description
00-15	MBC[15-0]	Monitor Block Count. These bits indicate the number of Monitor Blocks to log.

Monitor Block Counter Register

5.2.12 Monitor Filter Hi Register

Address: 001C (H)
Read/Write

The Monitor Filter Hi Register determines which RTs (RT 31 through RT 16) the module will monitor.

Bit	Bit Name	Description
00-15	MFH[31-16]	Monitor Filter. These bits determine which RT to monitor.

Monitor Filter Hi Register

5.2.13 Monitor Filter Hi Register

Address: 001E (H)
Read/Write

The Monitor Filter Lo Register determines which RTs (RT 15 through RT 0) the module will monitor.

Bit	Bit Name	Description
00-15	MFH[31-16]	Monitor Filter. These bits determine which RT to monitor.

Monitor Filter Hi Register

5.3 Bus Monitor Architecture

To meet the MIL-STD-1553 monitor requirements, the module uses a Monitor Block architecture that takes advantage of both Control Registers and RAM. The Monitor Block, that is located in contiguous memory, requires eight 16-bit locations for each message.

These eight locations include:

- A Message Information Word
- Two Command Word locations
- A Data Pointer
- Two Status Word locations
- A Time-Tag location
- A reserved location

The user must initialize the starting locations of the Monitor Block, the Data Pointer, the Block Counter, and the Interrupt Log Pointer. From then on, the module will build a Monitor Block for each message it receives over the 1553 bus. Figure 5-2 shows a diagram of the Monitor Block followed by a description of each location associated with the Monitor Block.

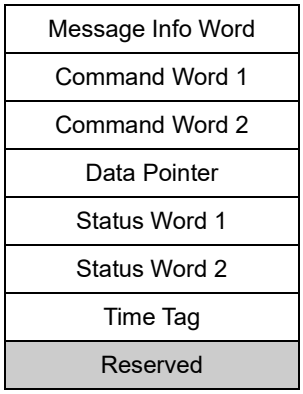

Figure 5-2 Bus Monitor Block Diagram

5.3.1 Message Information Word

The first memory location of each Monitor Block contains the message information word. Each information word contains the opcode, retry number, bus definition, RT-to-RT messages, and the message information.

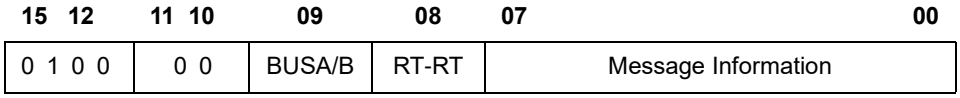

Figure 5-3 Message Information Word

Bit Number	Description
12-15	Default. With the Monitor Block architecture resembling the BC Command Block architecture, these bits default to a 0100 state (which is the Execute and Continue opcode) in case the monitor must switch to the BC mode of operation.
10-11	Default. With the Monitor Block architecture resembling the BC, these bits default to a '00' state. If the monitor must switch to the BC, the retries will be set at four per message.
09	Bus A/B. This bit defines on which of the two buses the command was received. (Logic 1 = Bus A, Logic 0 = Bus B).
08	RT-to-RT Transfer. This bit defines whether or not the message associated with this Monitor Block was an RT-to-RT transfer and whether the module saved the second command word. This bit will be set only if the module is instructed to monitor the Receive RT.
00-07	**Message Information Bits.** These bits define the conditions of the message received by the module for that particular Monitor Block. In an RT-to-RT transfer, the information applies to the complete message:
07	Message Error. This bit will be set if the monitor detects an error in either the Command Word, Data Words, or the RT's status.
06	Mode Code without Data. This bit will be set if the monitor detects that the command being processed is a mode code without data words.
05	Broadcast. This bit will be set if the monitor detects that the command being processed, is a broadcast message.
04	Reserved
03	Time-Out Error. This bit will be set if the RT did not receive the proper number of Data Words, e.g., the number of Data Words received was less than the word count specified in the Command Word.
02	Overrun Error. This bit will be set if the RT received a word when none were expected or the number of Data Words received was greater than expected.
01	Parity Error. This bit will be set if a parity error has occurred on the Data Words or the RT's status word.
00	Manchester Error. This bit will be set if a Manchester error has occurred on either the Data Words or the RT's status word.

Message Information Word

5.3.2 Command Words

The next two locations in the module Monitor Block are for Command Words. In non-RT-to-RT 1553 messages, only the first Command Word will be stored. However, in an RT-to-RT transfer, the first command word is the Receive Command and the second Command Word is the Transmit Command.

5.3.3 Data Pointer

The fourth location in the Monitor Block is the Data Pointer. This pointer points to the first memory location to store the Data Words associated with the message for this block. The data associated with each individual message will be stored contiguously. This data structure allows the module to store the specified number of data words.

Note In an RT-to-RT transfer, the BM uses the Data Pointer as the location in memory to store the transmitting data in the transfer.

5.3.4 Status Words

The next two locations in the Monitor Block are for Status Words. As the RT responds to the BC's command, the corresponding Status Word will be stored in Status Word 1. However, in an RT-to-RT transfer, the first status word will be the status of the Transmitting RT while the second Status Word will be the status of the Receiving RT.

5.3.5 Time Tag

The seventh location in the Monitor Block is the Time Tag associated with the message. The Time Tag is stored into this location at the end of message processing (i.e., captured after the command is validated).

5.3.6 Reserved

The last location in the Monitor Block is reserved.

5.4 Bus Monitor Block Chaining

The host determines the first Monitor Block by setting the start address in the Initial Monitor Block Pointer Register. Figure 5-4 shows the Monitor Block as the blocks execute in a contiguous fashion.

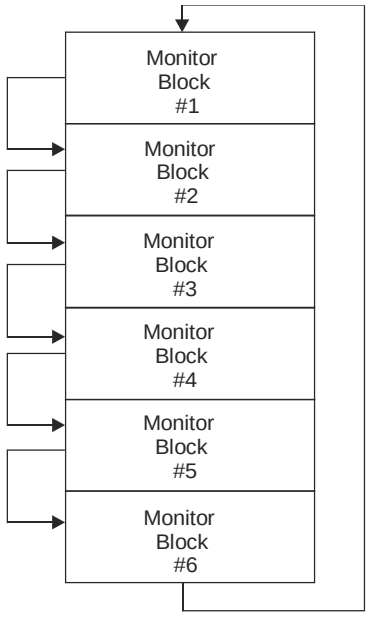

Figure 5-4 Bus Monitor Block Structuring

5.5 Memory Architecture

The configuration shows the Monitor Blocks, data locations and the Interrupt Log List as separate entities. Figure 5-5 shows that the first block of memory is allocated for the Monitor Blocks. Notice that the Initial Monitor Block Pointer Register points to the initial Monitor Block location, the Initial Monitor Data Pointer Register points to the initial Data location, Interrupt Log List Pointer Register points to the Interrupt Log, and the Monitor Block Counter Register contains the Monitor Block count. After execution begins, the module will build command blocks and store Data Words until the count reaches 0. When the count reaches 0, the module will simply wrap back to the initial values and start again.

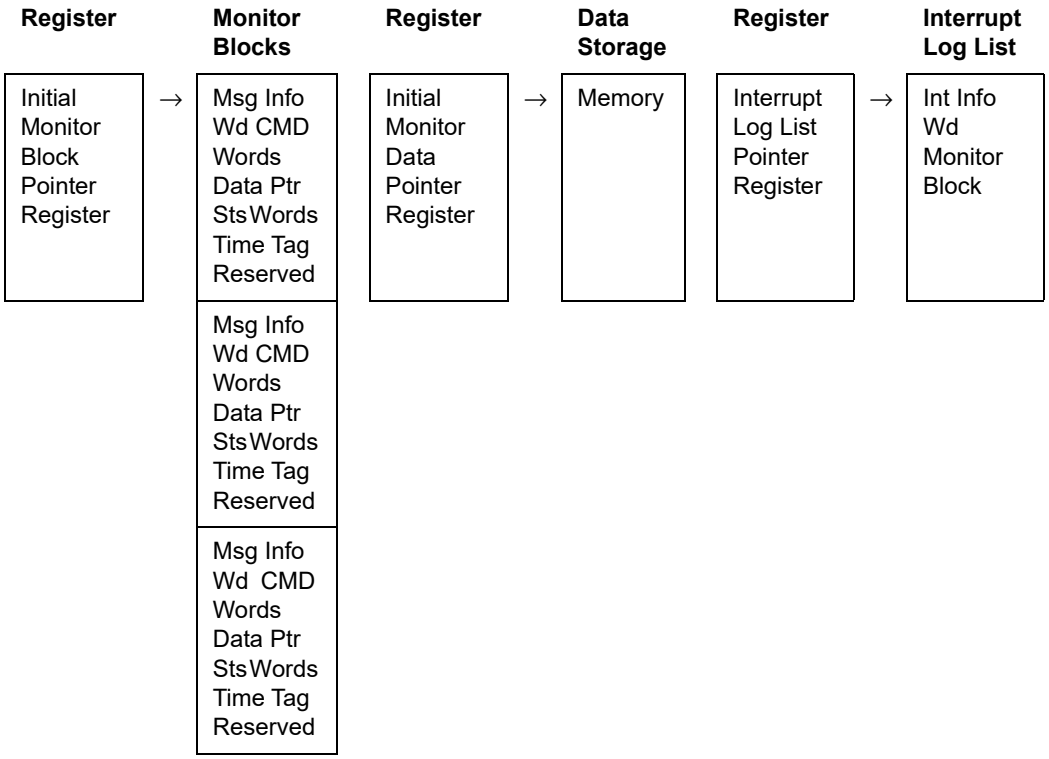

Figure 5-5 Memory Architecture for Bus Monitor Mode

5.6 RT/Concurrent Monitor Operation

For applications that require simultaneous Remote Terminal and Bus Monitor operation, the module should be configured as both a Remote Terminal and Bus Monitor. This feature allows the RT to communicate on the bus for one specific address and to monitor the bus for other specific addresses. Configuration as both Bus Monitor and RT precludes the module from monitoring its own Remote Terminal address.

When the module is configured as both RT and Bus Monitor, the RT has priority over the Bus Monitor. For example, commands to the RT will always take priority over commands for the Bus Monitor. The examples below describe what happens if the RT is defined for terminal address 1 and the Bus Monitor is to monitor terminal address 12.

Example 1:

Bus A	CMD/TA = 12
Bus B	CMD/TA = 1

In this example, the Bus Monitor will decode the first command on bus A, realize the message is for terminal address 12, and start monitoring the message. However, as soon as the module realizes the second command on bus B is to terminal address 1, the RT will take priority and begin RT message processing.

Example 2:

Bus A	CMD/TA = 1
Bus B	CMD/TA = 12

In Example 2, the RT will decode the first command on bus A, realize the message is for terminal address 1, and start message processing. As the message on bus B is received, the module will realize it is to terminal address 12, but since the RT has priority, the Bus Monitor will not switch to the bus monitor mode.

The above examples also apply to an RT-to-RT message. For example, if the first command in an RT-to-RT transfer matches the terminal address of the RT, the entire message will be stored (Message 1). However, if the first command in an RT-to-RT transfer matches the terminal address of the Bus Monitor and the second command matches the terminal address of the RT, the RT will take priority and only the RT message is stored (Message 2). Below is an RT-to-RT message example.

Message 1	CMD/TA = 1	CMD/TA = 12
Message 2	CMD/TA = 12	CMD/TA = 1

5.7 MIL-STD-1553A/B Operation: BM Mode

To maximize flexibility, the *M8K1553MCH* can operate in many different systems that use various protocols. Specifically, two of the protocols that the module may be used with are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, configure the module through the Control register (ERTO Bit 09) and the Operational Status register (A/B_STD Bit 07).

Table 5-1 defines the four ways to program the *M8K1553MCH*.

A/B_STD	ERTO	RESULT
0	0	1553B standard, 1553B response (in 14 μsec.)
0	1	1553B standard, extended response (in 30 μsec.)
1	0	1553A standard, 1553A response (in 9 μsec.)
1	1	1553A standard, extended response (in 21 μsec.)

Table 5-1: MIL-STD-1553A/B Operation: BC Mode

When configured as a MIL-STD-1553A bus controller, the *M8K1553MCH* will operate as follows:

- Looks for the RT response within 9 μsec.
- Ignores the T/R bit for all mode codes
- Defines all mode codes without data
- defines subaddress 00000 as a mode code

6 Module Interrupt Architecture

Chapter 6 describes the module interrupt architecture. The topics covered are:

6.1 Overview

The *M8K1553MCH* interrupt architecture involves three Control Registers, an Interrupt Log List, and the interrupt line. The three Control Registers include a Pending Interrupt Register, Interrupt Mask Register, and Interrupt Log List Register. The Pending Interrupt Register contains information that identifies the events generating the interrupts. The Interrupt Mask Register allows the user to mask or disable the generation of interrupts. The Interrupt Log List Register contains the base address of a 32-word interrupt ring buffer.

The lower twelve interrupt bits of the Pending Interrupt Register are entered into the Interrupt Log List, if the Interrupt Log List is enabled.

The interrupt architecture allows for the entry of 16 interrupts into a 32-word ring buffer. The *M8K1553MCH* automatically handles the interrupt logging overhead. Each interrupt generates two words of information to assist the host in performing interrupt processing. The Interrupt Identification Word (IIW) identifies the type(s) of interrupt that occurred. The Interrupt Address Word (IAW) identifies the interrupt source (e.g., subaddress or command block) via a 16-bit address.

6.1.1 Interrupt Identification Word (IIW)

The Interrupt Identification Word is a 16-bit word identifying the interrupt type. The format is similar to the Pending Interrupt Register. The host reads the IIW to determine which interrupt event occurred. The bit description for the IIW is provided below.

Bit	Bit Name	Description
12-15	Reserved	Set to 0
11	MERR	Message Error Interrupt (All modes)
10	SUBAD	Subaddress Accessed Interrupt (RT Mode)
09	BDRCV	Broadcast Command Received Interrupt (RT Mode)
08	IXEQ0	Index Equal Zero Interrupt (RT Mode)
07	ILCMD	Illegal Command Interrupt (RT Mode)
06	Reserved	Set to 0
05	EOL	End Of List (BC Mode)
04	ILLCMD	Illogical Command (BC Mode)
03	ILLOP	Illogical Opcode (BC Mode)
02	RTF	Retry Fail (BC Mode)
01	CBA	Command Block Accessed (BC Mode)
00	MBC	Monitor Block Count Equal Zero (BM Mode)

Interrupt Identification Word (IIW)

6.1.2 Interrupt Address Word (IAW)

The Interrupt Address Word is a 16-bit word that identifies the interrupt source. Depending on the mode of operation (i.e., RT, BC, or BM), the IAW has different meanings. In the RT mode operation, the IAW identifies the subaddress or mode code descriptor that generated the interrupt. For the BC mode of operation, the IAW points to the command block addressed when the interrupt occurred. In the BM mode of operation, the IAW marks the monitor counter count when the interrupt occurred. Use the IAW with the Initial Monitor Command Block Pointer Register to determine the monitor command block that generates the interrupt.

When in RT/Concurrent-BM mode, the user determines if the IAW contains information for the RT or the BM. The determination is made by comparing the contents of the IAW base address with the descriptor base address. If a match occurs, then the IAW contains a subaddress or mode code identifier. If no match occurs, the IAW contains monitor counter information.

6.1.3 Interrupt Log List Address

The Interrupt Log List resides in a 32-word ring buffer. The host defines the location buffer, within the memory space, via the Interrupt Log List Register. Restrict the ring buffer address to a 32-word boundary.

During initialization write a value to the Interrupt Log List Pointer Register. Initialize the least significant five bits to a logic 0. The most significant 11 bits determine the base address of the buffer. The module increments the ring buffer pointer on the occurrence of the first interrupt, storing the IIW and IAW at buffer locations 00 (H) and 02 (H) respectively. The module logs ensuing interrupts sequentially into the ring buffer until interrupt number 16 occurs. The module enters interrupt 16's IIW in buffer location 3C (H) and the IAW at location 3E (H).

The module increments the ring buffer pointer as interrupts occur. The least significant five bits of the Interrupt Log List Pointer register reflect the ring buffer pointer value. Table 6-1 shows the ring buffer architecture.

The user reads the ring buffer pointer value to determine the number of interrupts that have occurred. By extracting, the least significant five bits from the Interrupt Log List Register, and logical shifting the data once to the right, the host determines the number of interrupt events.

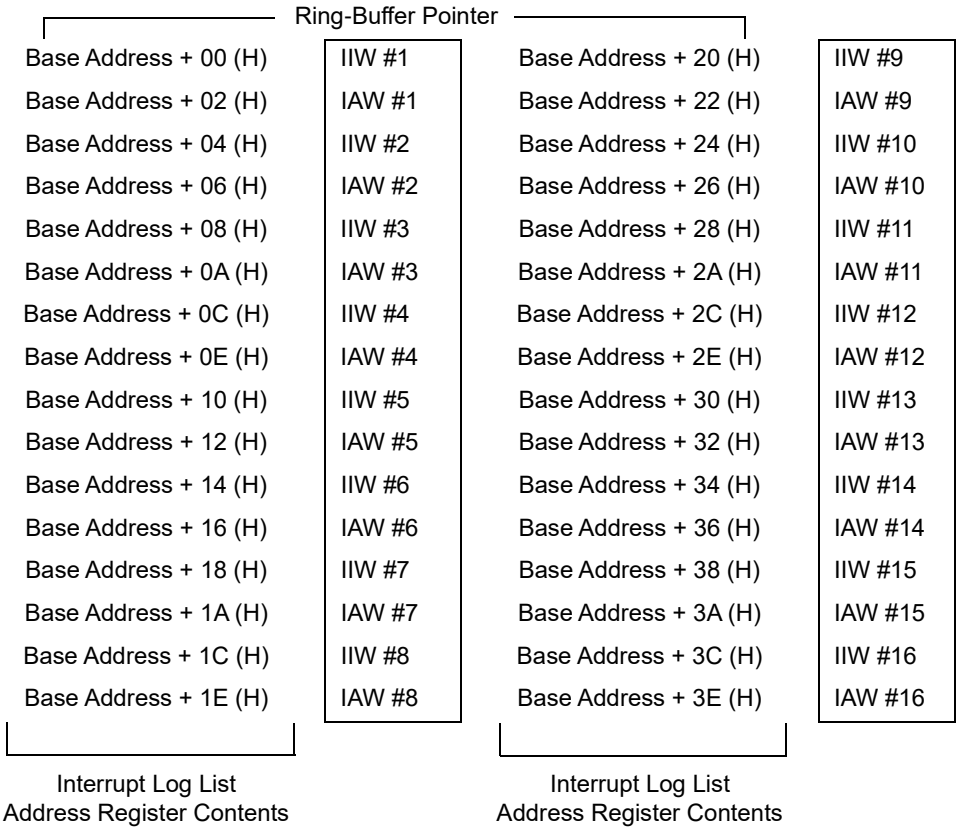

Table 6-1: Interrupt Ring Buffer

7 Mechanical And Electrical Specifications

Chapter 7 describes the mechanical and electrical specifications of the *M8K1553MCH*. The topics discussed are:

7.1 Module Layout

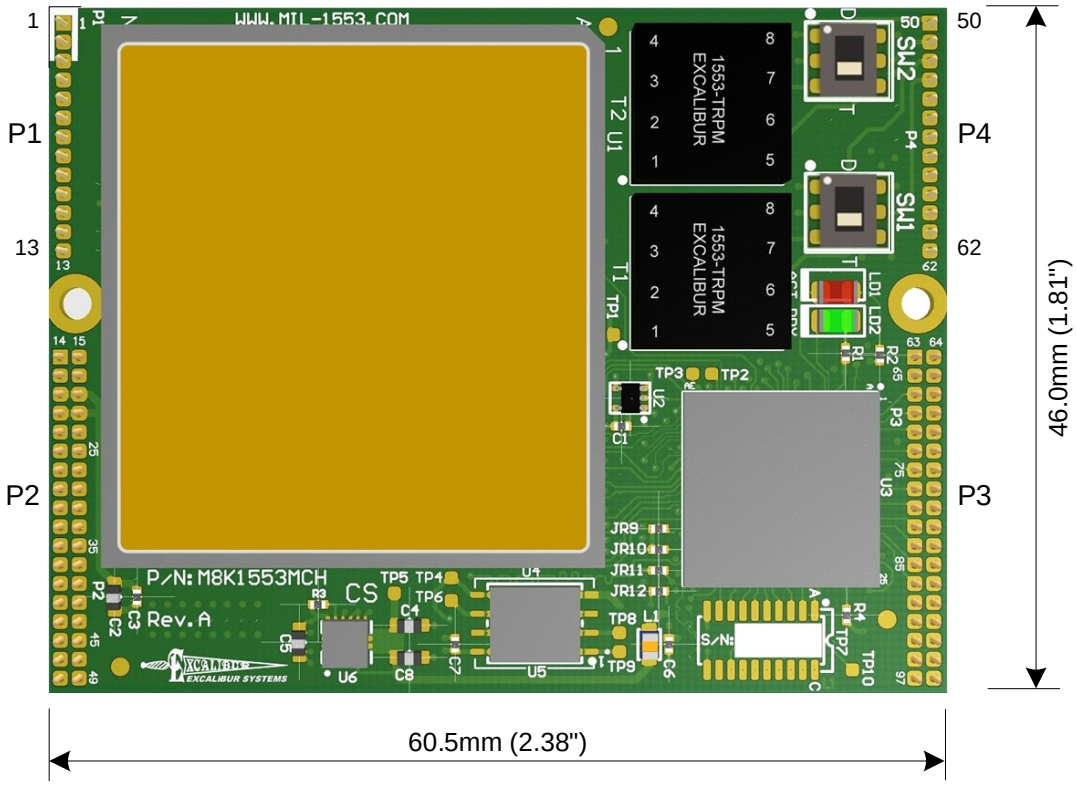

Figure 7-1 ***M8K1553MCH*** **Module Layout – Top View**

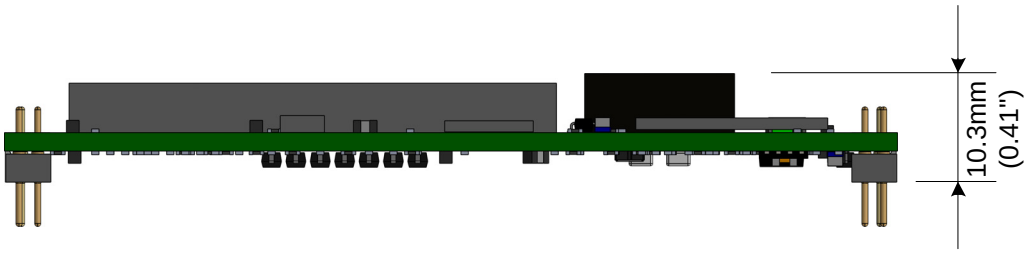

Figure 7-2 ***M8K1553MCH*** **Module Layout – Side View**

7.2 LED Indicators

The *M8K1553MCH* module contains two LEDs. The LEDs indicate operational mode and bus activity. The function of each LED is described below:

LED	Color	Indication
LD1	**Red**	Ready
LD2	**Green**	1553 message is being processed by the module

Table 7-1: Led Indicators

7.3 Module Coupling Mode DIP Switches [SW1–SW2]

The module can be either direct-coupled or transformer-coupled to the 1553 bus. DIP switches are used to select the coupling mode for each bus.

Table 7-2 defines the DIP switch settings.

Coupling Mode	Setting
Direct-Coupled	D
Transformer-Coupled	T

Table 7-2: Switch Settings Required to Select Coupling Mode

Table 7-3 defines the DIP switch for each bus:

Bus	DIP Switch
A	SW1
B	SW2

Table 7-3: Bus DIP Switch

Example: To set Bus A to transformer-coupled, switch SW1 to T.

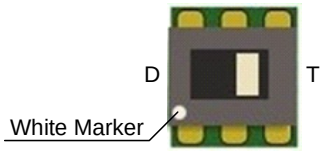

Figure 7-3 DIP Switch – Top View

7.3.1 Factory Default DIP Switch settings

The factory default settings are:

DIP Switch	Setting	Coupling Mode
SW1 (Bus A)	T	Transformer Coupled
SW2 (Bus B)	T	Transformer Coupled

Table 7-4: Factory Default DIP Switch Settings

7.4 Connectors

The module contains four 0.05" spacing strips (P1–P4), which comprise a total of 98 pins for all module connections. These pins mate with the carrier board socket strips. Out of these 98 pins, 12 pins are assigned for the communication I/O signals, pins 1–6 of connector P1 and pins 50–55 of connector P4. See Figure 7-1 on page 7-2.

On the *EXC-8000PCIe* and *EXC-8000PCIeHC* carrier boards, all the module's 12 I/O signals are wired to a 160-pin female connector. For the pinouts of the carrier board's 160-pin connector, and for the pinouts of the optional adapter cable, refer to the user's manual of the carrier board.

For the *EXC-8000PCIe104* carrier board, refer to the **Mechanical and Electrical** chapter of the *EXC-8000PCIe104 User's Manual*.

7.4.1 Module Pin Assignments

Pins 1–6 of connector P1 and pins 50–55 of connector P4 transfer the module's 12 I/O signals. See Figure 7-1 on page 7-2.

P1 Pin #	Signal Name	Description
1	RTA4	Reserved for RT address bit position 4 input
2	RTA3	Reserved for RT address bit position 3 input
3	RTA2	Reserved for RT address bit position 2 input
4	RTA1	Reserved for RT address bit position 1 input
5	RTA0	Reserved for RT address bit position 0 input
6	RTAPTY	Reserved for RT address parity bit input
P4 Pin #		
50	BUSBLO	Bus B connection Low
51	BUSBHI	Bus B connection High
52	BUSALO	Bus A connection Low
53	BUSAHI	Bus A connection High
54	RTLOCKn	Reserved for RT address lock input 0 = RT number locked (RT address is set to the value represented by pins 1 – 6) 1 = RT number unlocked (RT address can be changed by writing to the Operational Status Register)
55	GND	Provided for RT address pins that need to be set to '0'

Table 7-5 Module Pin Assignments

Note A double-sized module shares its I/O pins between the pins of two single module locations. For example, the module's P1 connector resides on module location 1's P1 connector, while the module's P4 connector resides on module location 0's P4 connector.

7.5 Power Requirements

The power requirements for each *M8K1553MCH* module that is installed on the carrier board are:

+5V @ 260mA (0% duty cycle: non-transmitting on 1553 bus)

+5V @ 460mA (25% duty cycle: transmitting on 1553 bus)

+5V @ 620mA (50% duty cycle: transmitting on 1553 bus)

+5V @ 860mA (87.5% duty cycle: transmitting on 1553 bus)

Example: The maximum power requirements for a 2 modules installed on the carrier board (@ 25% duty cycle per module) will be:

+5V @460mA x 2 = 920mA

8 Ordering Information

Chapter 8 explains how to indicate the options you want when ordering a *M8K1553MCH* module.

Basic Part #	Option	Description
M8K1553MCH		Single function MIL-STD-1553 double-sized interface module for the EXC-8000 family of carrier board. Operates as a single RT, BC, RT/Concurrent-BM or BM.
	-E	Add this suffix for extended temperature (-40° – +85°C) option.
	-R	Add this suffix for ruggedized option, with high components bonded.
	-001	Add this suffix for conformal coating option.

Appendix A MIL-STD-1553 Word Formats

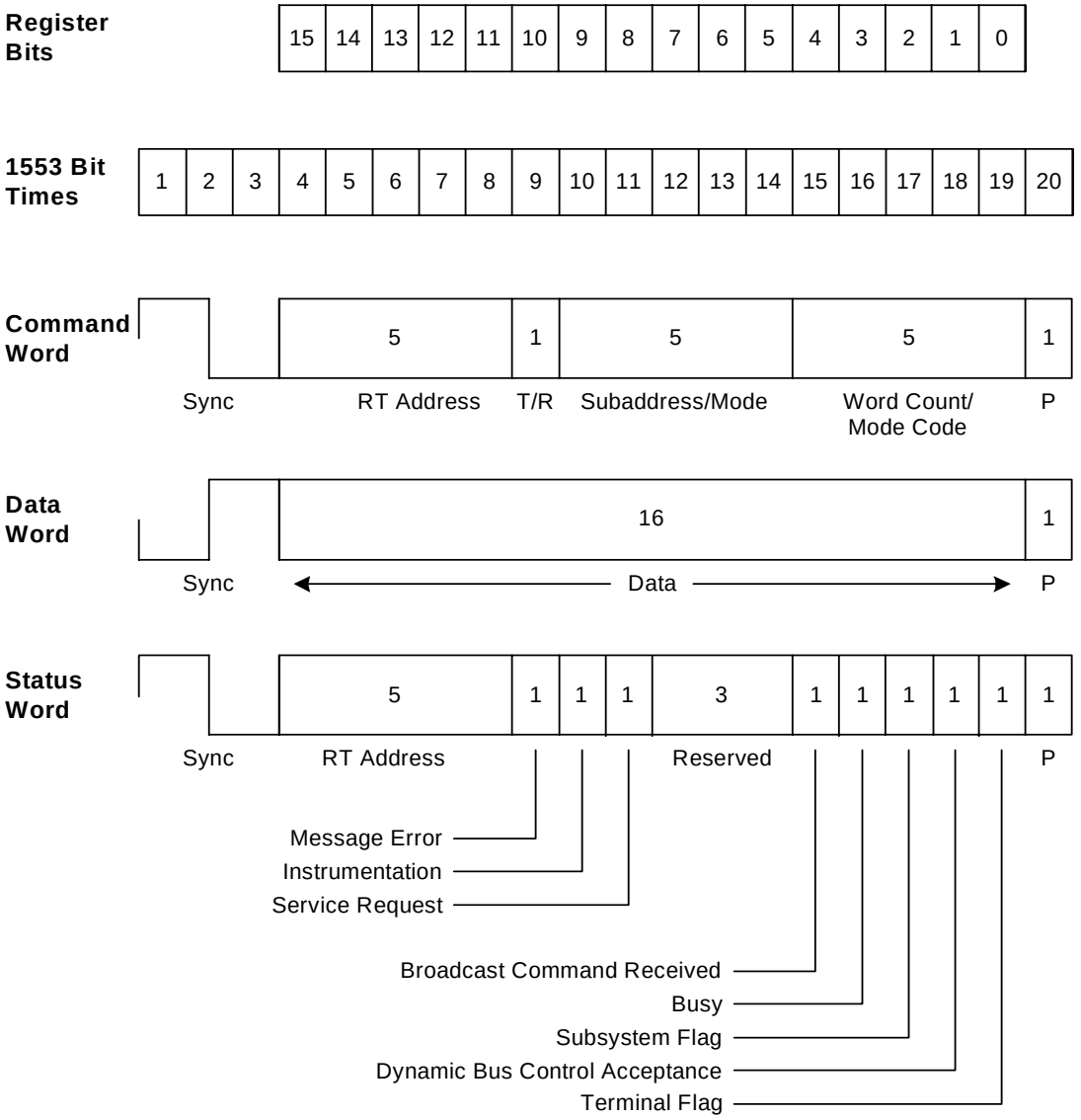

Figure A-1 MIL-STD-1553 Word Formats

Note: T/R = Transmit/Receive
P = Parity

Appendix B MIL-STD-1553 Message Formats

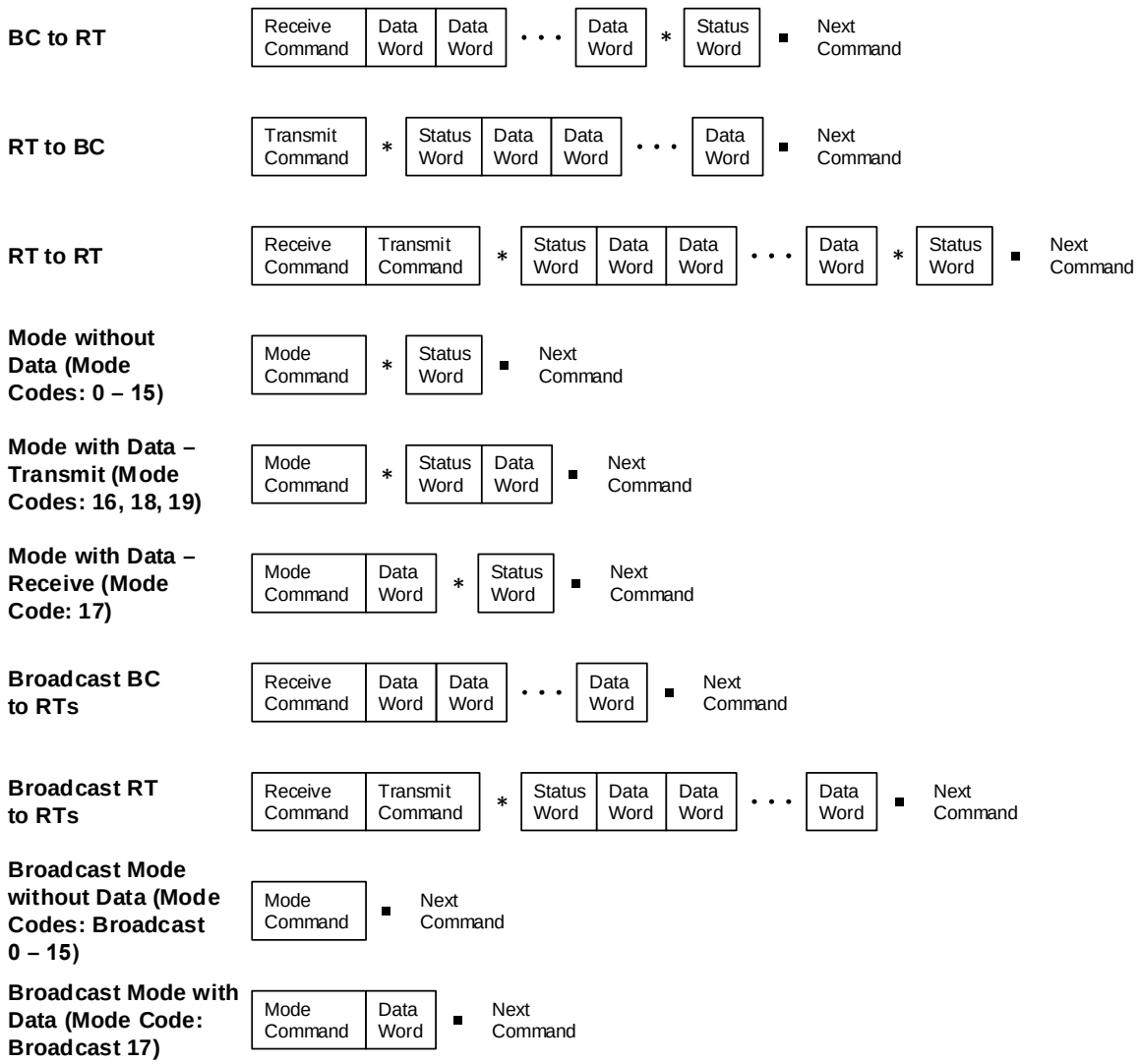

Figure B-1 MIL-STD-1553B Message Formats

Note: * = Response time
▪ = Intermessage Gap time

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