EXC-8000ccVPX

Test and Simulation Carrier Board for VPX Systems

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

The following topics are covered:

1.1 Overview

The *EXC-8000ccVPX* carrier board is a multiprotocol VPX interface board for avionics test and simulation applications. The board holds up to four removable modules, and comes with an onboard Discrete module. The four removable modules can be any one of the following types:

M8K429RT5	ARINC 429 multi-channel interface module. This module supports five ARINC 429 channels each of which can be configured in real time as a receive or transmit channel.
M8K708	ARINC 708 interface module. This module supports up to two ARINC 708/453 channels for the Weather Radar Display Databus. Each channel is selectable as transmit or receive and implements a 64K-word FIFO and supports polling and/or interrupt driven operation.
M8KH009	H009 interface module. This module supports a fully functional H009 channel (CCC, multi-PU,MON) and a concurrent Bus Monitor. This is a double-sized module and occupies two modules locations.
M8K717-Nx	ARINC 717 interface module. This module supports two ARINC 717 channels; one receive channel and one transmit channel.
M8K825CAN-S5	ARINC 825 interface module. This module supports up to five ARINC 825 channels.
M8KDiscrete	Discrete I/O interface module. This module supports 10 bi-directional Discretes with TTL (0 to 5 volts) or avionics (0 to 32 volts) voltage levels.
M8K1553Px	MIL-STD-1553 interface module. This module operates as a Bus Controller, up to 32 Remote Terminals and as a Bus Monitor. It supports an Internal Concurrent Monitor in RT and BC/RT modes.
M8K1553PxS	Same as the M8K1553Px, but for only one Remote Terminal at a time (single function) and one mode at a time (no BC/RT mode) and no error injection.
M8K1553PxM	Monitor-only version of the M8K1553Px.
M8K1553PxSM	Monitor-only version of the M8K1553PxS.
M8K1760Px	MIL-STD-1760 interface module. This module operates as a Bus Controller, up to 32 Remote Terminals and as a Bus Monitor. It supports an Internal Concurrent Monitor in RT and BC/RT modes.
M8K1760PxS	Same as the M8K1760Px, but for only one Remote Terminal at a time (single function) and one mode at a time (no BC/RT mode) and no error injection.
M8K1760PxM	Monitor-only version of the M8K1760Px.
M8K1760PxSM	Monitor-only version of the M8K1760PxS.
M8KMMSI-R5	Mini Munitions Store Interface module. This module supports RT, BC/ Concurrent-RT/ Concurrent Monitor and Bus Monitor modes. Up to 5 hub ports EBR-1553 (10 Mbps MIL-STD-1553 protocol using RS-485 transceivers) and a composite monitor output (cBM).
M8KSerial-Jx	Serial communications interface module. This module supports two independent channels of serial communications, each of which can be selected as RS485, RS422 or RS232.
M8KADDA	Multichannel digital-to-analog and analog-to-digital interface module. This module supports up to 10 single ended, or 5 differential, digital-to-analog (DAC) output channels, as well as 5 single ended or 5 differential analog-to-digital (ADC) input channels.

Excalibur will be adding modules to those listed above, increasing the board's flexibility even further.

You can choose to populate the board with different types of modules or with multiple modules of the same type. For example, populating the board with four *M8K429RT5* modules will give you *twenty* programmable channels. All modules come with Windows drivers, including source code.

1.1.1 Board Features

General Features

- Supported protocols (on up to 4 removable modules):
  - ARINC 429/575 (5 channels per module)
  - ARINC 708/453 (2 channels per module)
  - ARINC 717 (2 channels per module)
  - ARINC 825 (CAN) (5 channels per module)
  - MIL-STD-1553 (single or multifunction)
  - MIL-STD-1760 (single or multifunction)
  - H009 (double-sized module with one channel)
  - Discrete I/O (10 channels per module)
  - Serial RS-485/RS-422/RS-232 (2 channels per module)
  - MMSI/AS5652 (5 channels per module)
  - A/D and D/A (5 differential or 10 single ended channels)
- 16-bit Count Down Timer
  - 1–65,635 µs resolution
  - Interrupt or global reset upon count down

IRIG B Time Code Input

- Carrier wave:
  - 1KHz Amplitude modulated sine wave
- Rate Designation: 100 peaks per second
- Modulation ratio: 3:1
- Input Amplitude: 0.8–3.5 Vpp (3 Vpp Typ)
- Coded Expressions supported:
  - BCD time-of-year code word
  - Control functions
  - Straight Binary Seconds (SBS) time-of-day
- Application:
  - Synchronization of Time Tags, display and IRIG B time

Physical Characteristics

- Dimensions: Standard 3U size, 160 mm x 100 mm (not including frame or connectors)
- Weight: 232 g (without removable modules)

Operating Environment

- Temperature: 0°–70°C standard temperature
  -40° to +85°C extended temperature (optional)
- Humidity: 5%–90% noncondensing
- MTBF: 178,600 hours at 25°C, G_F, S217F

Host Interface

- PCI Express compliance: x1 lane PCIe v1.1
- Compatible with VITA 65 Peripheral Slot profile:
  SLT3 PER-1U-14.3.3 (x1 PCIe)
- Also compatible with:
  SLT3-PER-1F-14.3.2 (x4 PCIe)
  SLT3-PER-2F-14.3.1 (x8 PCIe)
  SLT3-PER-1Q-14.3.4 (x16 PCIe)
- Memory space occupied: 64 MB
- Interrupts: INTA# virtual wire
- Power: Depends on configuration. For more details, see **3.5 Power Requirements** on page 3-15.

Software Support

- *Excalibur Carrier Board Software Tools*:
  Intuitive and flexible API with source code
  Compatible with 32/64-bit Windows 7/8/10 & Linux kernel 3.x/4.x
  Includes application interface for NI LabView & CVI
- *Exalt Plus*: Excalibur Analysis Laboratory Tools for Windows (optional)

System Requirements

- Operating system: 64-bit Windows
- CPU: Intel® Core™ i3 Processors or equivalent (recommended)
- RAM: 8 GB (recommended)

1.1.2 Block Diagram

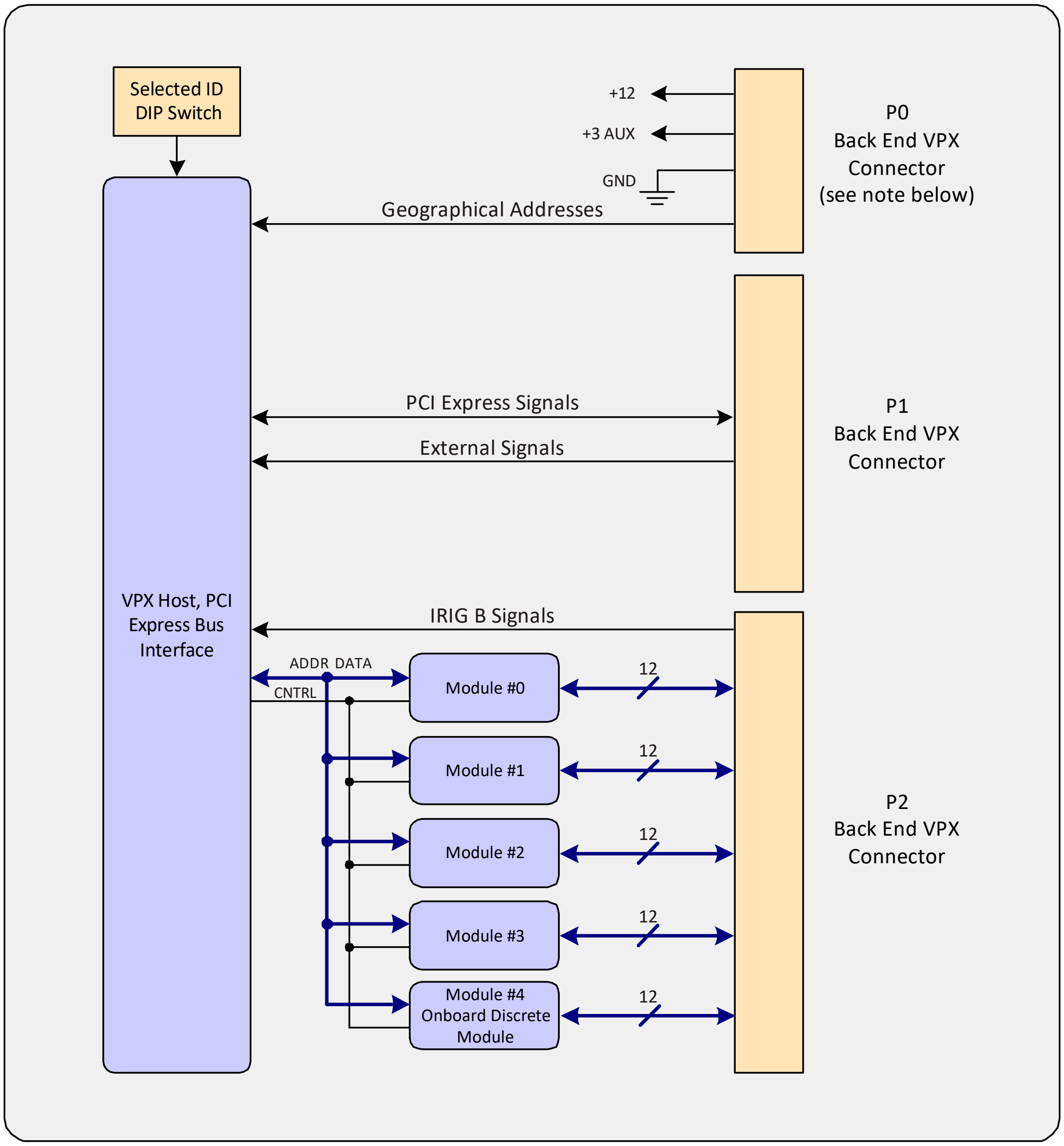

Figure 1-1 Block Diagram

Note: There is an option for legacy power (+5V/+3V supply). For more information, contact Excalibur Sales. See **1.3 Technical Support** on page 1-6.

1.2 Installation

For hardware and software installation instructions, see **Installation Instructions.pdf** in the root folder of the installation CD. When downloading new software from the Excalibur website, **Installation Instructions.pdf** is contained in the zip file.

The *Excalibur Installation CD* you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. For more details, see **Installation Instructions.pdf**. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.3 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, visit the Technical Support page of our website (www.mil-1553.com). You can also contact us by phone. To find the location nearest you, visit to the Contact Us page of our website. Before contacting Technical Support, please see Information Required for Technical Support.

2 PCI Architecture

Chapter 2 describes the PCI Express architecture. The following topics are covered:

2.1 Memory Structure

The *EXC-8000ccVPX* requests the following memory blocks:

- The first memory block (Base Address Register 0) is 64 MB and contains the memory space for the modules on the board. For more information, see **2.8 Module Memory Space Map** on page 2-18.
- The second memory block (Base Address Register 1) is 32 KB in size and contains the DMA registers. DMA functionality is described in the software tools programmer's reference of each of your board's modules.
- The third memory block (Base Address Register 2) is 8 KB in size and contains the Global registers. For more information, see **2.5 Board Global Registers Map** on page 2-9.

2.2 PCI Configuration Space Header

The board includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

The following figure shows the PCI Express Configuration Space Header for PCI Express:

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0s				38 H
Reserved = 0s			Cap. pointer	34 H
Expansion ROM Base Address (Not Used)				30 H
Subsystem ID		Subsystem Vendor ID		2C H
Cardbus CIS Pointer – Not Used = 0s				28 H
Base Address Register #5 – Not Used				24 H
Base Address Register #4 – Not Used				20 H
Base Address Register #3 – Reserved				1C H
Base Address Register #2 – Global Registers				18 H
Base Address Register #1 – DMA Registers				14 H
Base Address Register #0 – Module Memory Space				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status Register		Command Register		04 H
Device ID		Vendor ID		00 H
31 24	**23 16**	**15 08**	**07 00**	

Figure 2-1 PCI Configuration Space Header

2.3 PCI Configuration Registers

2.3.1 Vendor Identification Register (VID) — Address: 00–01 (H)

Power-up value 1405 H

Size: 16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems.

2.3.2 Device Identification Register (DID) — Address: 02–03 (H)

Power-up value: E850 H

Size: 16 bits

The Device Identification register contains the board's device identification number.

2.3.3 PCI Command Register (PCICMD) — Address: 04–05 (H)

Power-up value: 0000 H

Size: 16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0s
09	**Fast Back-to Back Enable**	Always set to 0
08	**System Error Enable**	Always set to 0
07	**Address Stepping Support**	Always set to 0
06	**Parity Error Enable**	Always set to 0
05	**VGA Palette Snoop Enable**	Always set to 0
04	**Memory Write and Invalidate Enable**	Always set to 0
03	**Special Cycle Enable**	Always set to 0
02	**Bus Master Enable**	Always set to 1
01	**Memory Access Enable**	Always set to 1
00	**I/O Access Enable**	Since the board does not use I/O space, the value of this register is ignored.

Table 2-1 PCI Command Register

2.3.4 PCI Status Register (PCISTS) — Address: 06–07 (H)

Power-up value: 0080 H

Size: 16 bits

The PCI Status register contains the PCI status information for PCI Express.

Bit	Bit Name	Description
15	**Detected Parity Error**	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	**Signaled System Error**	Not used
13	**Received Master Abort**	This bit is set when the device receives a master abort to terminate a transaction. This bit can be reset by writing a 1 to this location.
12	**Received Target Abort**	Not used
11	**Signaled Target Abort**	Not used
09-10	**Device Select (DEVSEL#) Timing Status**	Set to 00 (fast timing)
08	**Data Parity Reported**	Not used
07	**Fast Back-to-Back Capable**	Set to 0
06	**UDF Supported**	Set to 0
05	**66MHz capable**	Set to 0
04	**Capability List enable**	Set to 1
03	**Interrupt Status**	This bit is set when an interrupt is received.
00-02	**Reserved**	

Table 2-2 PCI Status Register

2.3.5 Revision Identification Register (RID) — Address: 08 (H)

Power-up value: 01 H

Size: 8 bits

The Revision Identification register contains the revision identification number of the board.

2.3.6 Class Code Register (CLCD) — Address: 09–-0B (H)

Power-up value: FF0000 H

Size: 24 bits

The Class code Register value indicates that the board does not fit into any of the defined class codes.

2.3.7 Cache Line Register Size Register (CALN) — Address: 0C (H)

Power-up value: 10 H

Size: 8 bits

Not used

2.3.8 Latency Timer Register (LAT) — Address: 0D (H)

Power-up value: 00 H

Size: 8 bits

Not used

2.3.9 Header Type Register (HDR) — Address: 0E (H)

Power-up value: 00 H

Size: 8 bits

The board is a single function PCI device.

2.3.10 Built-In Self-Test Register (BIST) — Address: 0F (H)

Power-up value: 00 H

Size: 8 bits

The Built-In Self-Test register is not implemented in the board.

2.3.11 Base Address Registers (BADR) — Address: 10, 14, 18, 1C, 20, 24 (H)

Power-up value: 00000000 H for each

Size: 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

Three memory pages are required by the board: one for the module memory space, one for the Global Registers and one for the DMA registers.

Register	Offset	Size	Function
Base Address 0	10 H	64 MB	Module memory space
Base Address 1	14 H	32 KB	DMA registers
Base Address 2	18 H	8 KB	Global registers

Table 2-3 Base Address Registers Definition

Note: Each Base Address Register contains 32 bits. Since the PCI Express board uses 64-bit address space, each memory page covers two base addresses (0 – 1, 2 – 3, 4 – 5).

The following table describes the bits of the Base Address Register.

Bit	Description
04-31	Address of memory region (with lower 4 bits removed)
03	Always 1 – memory is prefetchable
01-02	Always 2 – memory may be mapped anywhere within the 64 bit memory space
00	Always 0 – indicates memory space

Table 2-4 Base Address Register

2.3.12 Cardbus CIS Pointer — Address: 28 (H)

Power-up value: 00000000 H

Size: 32 bits

The Cardbus Pointer is not implemented on the board.

2.3.13 Subsystem ID — Address: 2C (H)

Power-up value: 0000 H

Size: 16 bits

2.3.14 Subvendor ID — Address: 2E (H)

Power-up value: 0000 H

Size: 16 bits

2.3.15 Expansion ROM Base Address Register (XROM) — Address: 30 (H)

Power-up value: 00000000 H

Size: 32 bits

The Expansion ROM Space is not implemented on the board.

2.3.16 PCI Capabilities Pointer — Address: 34 (H)

Power-up value: 50 H

Size: 8 bits

The PCI Capabilities Pointer (Cap. Pointer) indicates the location of the PCI Capabilities Identification (ID) Register. The Capabilities ID Register stores a pointer to a structure within the configuration space. With a known Capabilities ID value, the associated structure can be found during the scanning process.

2.3.17 Interrupt Line Register (INTLN) — Address: 3C (H)

Power-up value: 00 H

Size: 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 1 to F (H) correspond with the IRQ numbers 1 through 15, and the values from 10(H) to FE (H) are reserved. The value of 255 signifies either “unknown” or “no connection” for the system interrupt.

2.3.18 Interrupt Pin Register (INTPIN) — Address: 3D (H)

Power-up value: 01 H

Size: 8 bits

Set to INTA#

2.3.19 Minimum Grant Register (MINGNT) — Address: 3E (H)

Power-up value: 00 H

Size: 8 bits

The Minimum Grant register is not implemented on the board.

2.3.20 Maximum Latency Register (MAXLAT) — Address: 3F (H)

Power-up value: 00 H

Size: 8 bits

The Maximum Latency register is not implemented on the board.

2.4 Board Global and DMA Registers Memory Space Map

The DMA Registers are mapped as follows.

DMA Registers	7FFF H 0000 H

Figure 2-2 DMA Registers Memory Space Map

The Global Registers are mapped as follows.

Reserved	1FFF H 1000 H
Global Registers	0FFF H 0000 H

Figure 2-3 Global Registers Memory Space Map

2.5 Board Global Registers Map

The board global registers reside in the second memory block.

Register (Bit No. 15 … 0)	Address
Reserved	A2–0FFF H
Geographical Address	A0 H
Reserved	3A–9E H
Module 4 Info	38 H
Reserved	30–36 H
General Purpose Timer	28 H
Reserved | Timer Control	26 H
Timer Preload	24 H
Timer Prescale	22 H
FPGA Revision	20 H
Control Functions Low	1E H
Reserved | Control Functions Hi	1C H
(Reserved) | IRIG B Time Minutes | (Reserved) | IRIG B Time Seconds	1A H
IRIG B Time Days | IRIG B Time Hours	18 H
IRIG B Time SBS Low	16 H
Reserved | Sync IRIG B | Reserved | SBS Hi[1]	14 H
Reserved	12 H
Time Tag Clock Select	10 H
Module 3 Info	0E H
Module 2 Info	0C H
Module 1 Info	0A H
Module 0 Info	08 H
Interrupt Reset	06 H
Interrupt Status	04 H
Software Reset	02 H
Board ID	00 H

Bit No. 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Figure 2-4 Global and IRIG B Registers Map

1. IRIG B Time SBS Hi Register

2.5.1 Board Identification Register

Address: 00 (H)
Length 16 bits

Read only The Board Identification register comprises the following identification items.

Bit	Description
04-15	Hard coded to the value 8E0 H
00-03	Selected ID See **3.3.1 Select ID DIP Switch [SW1]** on page 3-2.

Table 2-5 Board Identification Register

2.5.2 Software Reset Register

Address: 02 (H)
Length 16 bits

Read/Write The Software Reset register performs reset operations of the modules. Individual modules may be reset.

Bit 04, the Global Time Tag reset bit, resets all the module's Time Tag counters.

Bit	Description	
06-15	Reserved – set to 0	
05	Module 4 reset	1 = reset module 0 = no effect
04	Global time tag reset	1 = reset all time tag counters 0 = no effect
03	Module 3 reset	1 = reset module 0 = no effect
02	Module 2 reset	1 = reset module 0 = no effect
01	Module 1 reset	1 = reset module 0 = no effect
00	Module 0 reset	1 = reset module 0 = no effect

Table 2-6 Software Reset Register

2.5.3 Interrupt Status Register

Address: **04 (H)**
Length **16 bits**

Read only The Interrupt Status register indicates which modules are currently interrupting or if the General Purpose Timer has produced an interrupt.

Bit	Description
06-15	Reserved – set to 0
05	1 = indicates that module 4 is interrupting
04	1 = indicates that an interrupt was generated by the General Purpose Timer [See **2.7 Global Timer Registers** on page 2-16]
03	1 = indicates that module 3 is interrupting
02	1 = indicates that module 2 is interrupting
01	1 = indicates that module 1 is interrupting
00	1 = indicates that module 0 is interrupting

Table 2-7 Interrupt Status Register

2.5.4 Interrupt Reset Register

Address: **06 (H)**
Length **16 bits**

Write only The Interrupt Reset register resets the interrupting modules by writing to the relevant bits of the register.

Bit	Description
06-15	Reserved – set to 0
05	1 = Resets module 4 interrupt 0 = No effect
04	1 = Resets General Purpose Timer interrupt 0 = No effect
03	1 = Resets module 3 interrupt 0 = No effect
02	1 = Resets module 2 interrupt 0 = No effect
01	1 = Resets module 1 interrupt 0 = No effect
00	1 = Resets module 0 interrupt 0 = No effect

Table 2-8 Interrupt Reset Register

2.5.5 Module Info Registers for Modules 0 – 3

Address: **08, 0A, 0C, 0E (H)**
Length **16 bits each**

Read only The Module Info Registers provide identification information for each of the modules.

Bit	Description	
12-15	Module number	00 H = Module 0 Info register 01 H = Module 1 Info register 02 H = Module 2 Info register 03 H = Module 3 Info register
08-11	Reserved – set to 0	
00-07	Module type	24 H = *M8K429RT5* module 25 H = *M8K1553Px* or *M8K1760Px* module 26 H = *M8KMMSI* module 27 H = *M8K708* module 28 H = *M8K825CAN* module 29 H = *M8KH009* module 2A H = *M8KADDA* module 2D H = *M8KDiscrete* module 32 H = *M8KSerial* module 37 H = *M8K717* module 1F H = no module installed

Table 2-9 Module Info Registers

2.5.6 Module Info Register for Module 4

Address: **38 (H)**
Length **16 bits each**

Read only The Module Info Register provides identification information for module 4.

Bit	Description	
12-15	Module number	04 H = Module 4 Info register
08-11	Reserved – set to 0	
00-07	Module type	2D H = *M8KDiscrete* module

Table 2-10 Module Info Register

2.5.7 Time Tag Clock Select Register

Address: 10 (H)
Length 16 bits

Read/Write The Time Tag Clock Select Register is used to set either an internal (1 MHz) or external source for the board's Global Time Tag Clock. When using an External Time Tag, it is received via the EXTTCLKI pin of connector J1. See **3.4.2 PCI Express and External Signals Connector [P1]** on page 3-7.

Bit	Description	
01-15	Reserved – set to 0	
00	Time Tag Clock Select	1 = External Source 0 = Internal Source [**Default**]

Table 2-11 Time Tag Clock Select Register

2.5.8 FPGA Revision Register

Address: 20 (H)
Length 16 bits

Read only The FPGA Revision register contains the FPGA revision of the board.

2.6 IRIG B Global Registers

The *EXC-8000ccVPX* is able to receive and decode standard serial IRIG B time code format signals via connector J1. The signals are 1 KHz carrier wave, sine wave, amplitude modulated, 100 peaks per second. See the IRIG B signals in **3.4.3 Modules I/O Signals Connector [P2]** on page 3-9.

The IRIG B signal, which contains 3 types of words within each Time Code Frame, can be used to synchronize the Time Tags of the modules on the board.

1st Word Time-of-year in binary coded decimal (BCD) notation in hours, minutes and seconds.

2nd Word Set of bits reserved for decoding various control, identification and other special purpose functions.

3rd Word Seconds-of-day weighted in straight binary seconds (SBS) notation

These three words can be stored and displayed in the IRIG B global registers 14 - 1E (H).

See **Figure 2-4 Global and IRIG B Registers Map** on page 2-9 for the location of the registers on the memory map.

Note: The synchronization of IRIG B time can take up to two seconds. IRIG B functions are meant to be used on an occasional basis, not on a constant basis.

2.6.1 Sync IRIG B Register

Address: 14 (H)
Bits 08 – 10

Read/Write The 3-bit Sync IRIG B register controls the synchronization of a module's Time Tags relative to the IRIG B input signal and the display of the IRIG B time within the IRIG B time registers.

Bit	Description	
10	1	Set by board to indicate that the current IRIG B time has been stored in the IRIG B registers
	0	No IRIG B time has been stored in the IRIG B registers. This bit must be reset by the user after the board has written a '1'.
09	1	Stores and displays the IRIG B time and control functions into the 6 IRIG B registers (14-1E [H]) corresponding to the previous valid IRIG B message. If bit 08 is set, then the IRIG B time will be stored at the same time that the Time tags are reset. To calculate the realtime to which the Time tags are synchronized the user will need to **add** '1' to the value of the IRIG B time stored into these registers.
	0	The previous valid IRIG B message should not be stored in the IRIG B registers. This bit will be automatically reset by the board after the storage of the IRIG B time.
08	1	Resets and synchronizes Time Tags of all the modules to the next rising edge of the on-time Reference Point **Pr** of the IRIG B signal. Also sets Bit 09 to a value of '1' in order to store and display the IRIG B time and control functions into the 6 IRIG B registers.
	0	No reset/synchronization of Time tags relative to the **Pr** of the IRIG B signal. This bit will be automatically reset by board after reset of time tags

Table 2-12 Sync IRIGB Register

Note: All bits are read and write.

2.6.2 IRIG B Time SBS High Register

Address: 14 (H)
Bit 0

Read only The IRIG B Time SBS High register contains the MSB of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.6.3 IRIG B Time SBS Low Register

Address: 16 (H)
Bits 15 – 0

Read only The IRIG B Time SBS Low register contains the lower 16 bits of the 17 bit straight binary representation of the seconds-of-day code word within the IRIG B message.

2.6.4 IRIG B Time Days Register

Address: 18 (H)
Bits 15 – 6

Read only The IRIG B Time Days register contains the days value of the BCD time-of-year subword within the IRIG B coded message.

2.6.5 IRIG B Time Hours Register

Address: 18 (H)
Bits 5 – 0

Read only The IRIG B Time Hours register contains the hours value of the BCD time-of-year subword within the IRIG B coded message.

2.6.6 IRIG B Time Minutes Register

Address: 1A (H)
Bits 14 – 8

Read only The IRIG B Time Minutes register contains the minutes value of the BCD time-of-year subword within the IRIG B coded message.

2.6.7 IRIG B Time Seconds Register

Address: 1A (H)
Bits 6 – 0

Read only The IRIG B Time Seconds register contains the seconds value of the BCD time-of-year subword within the IRIG B coded message.

2.6.8 Control Functions Registers

Hi Register Address: 1C (H) / Bits 10 – 0
Low Register Address: 1E (H) / Bits 15 – 0

Read only The IRIG B time code formats reserve 27 bits known as Control Functions. The Control Functions are for user-defined encoding of various control, identification or other special purpose functions. No standard coding system exists. The control bits may be programmed in any predetermined coding system.

2.6.9 FPGA Revision Register

Address: 20 (H)
Bits 15 – 0

Read only The FPGA Revision register contains the FPGA revision of the board.

2.7 Global Timer Registers

See **Figure 2-4 Global and IRIG B Registers Map** on page 2-9 for location of the registers on the memory map.

2.7.1 Timer Prescale Register

Address: 22 (H)
Bits 15 – 0

Read/Write The Timer Prescale Register defines the resolution of the General Purpose Timer. It is based on the Global Time Tag Clock (nominally 1 MHz) and thus will give the General Purpose Timer resolution as follows:

Timer Prescale Register Value (DEC)	General Purpose Time Resolution (μsec)
0 or 1	1 (default)
2	2
3	3
•	•
•	•
•	•
10	10
•	•
•	•
•	•
65535	65535

Table 2-13 Timer Prescale/General Purpose Timer Resolution

Note: The Timer Prescale register can only be changed when the timer has been stopped.

2.7.2 Timer Preload Register

Address: 24 (H)
Bits 15 – 0

Read/Write The value stored in the Timer Preload Register sets the starting count value for the General Purpose Timer from which it will start to count down. The Timer Preload Register can only be changed while the timer is stopped and has a maximum count value of 65535.

Note: The General Purpose Timer will not start counting if a value of zero is stored into the Timer Preload Register.

Default value: 00 00

2.7.3 Timer Control Register

Address: 26 (H)
Bits 3 – 0

Read/Write The Timer Control Register is used to control the General Purpose Timer register. The value stored in bits 01 to 03 take effect when the General Purpose timer reaches a value of zero. Bit 00 is used to start and stop the General Purpose

Timer. The values of bits 01 – 03 can only be changed when the General Purpose Timer register is stopped.

Default value: 00 00

Bit	Description		
04-15	Reserved - set to 0		
03	Global reset on count completed	1 0	Causes global reset of all installed modules No effect
02	Interrupt on count completed	1 0	Output an interrupt (see **2.5.3 Interrupt Status Register** on page 2-11) No effect
01	Reload mode	1 0	Reload mode Non-reload/One-shot mode
00	Start/Stop	1 0	Start Stop

Table 2-14 Timer Control Register

2.7.4 General Purpose Timer Register

Address: 28 (H)
Bits 15 – 0

Read Only

The General Purpose Timer Register stores the current count value of the General Purpose Timer. The General Purpose Timer is controlled by the Timer Control Register. When the General Purpose Timer is started it will count down to zero, at which point either an interrupt can be generated and or all installed modules can be reset.

If the General Purpose Timer is in reload mode then the current value in Timer Preload Register will be stored into the General Purpose Timer and the timer will start to count down from this value.

If the General Purpose Timer is in non-reload / one shot mode, when it reaches zero it will stop and a value of zero will be displayed in the General Purpose Timer Register. In this case bit 00 (Start/Stop bit) of the Timer Control Register will automatically be set to zero in this case. If the General purpose Timer Register is then started it will start to count from the current Timer Preload Register value automatically (without the need to do a write to the Timer Preload Register).

At any point in time, the General Purpose Timer can be stopped at the current count value. When a start is then issued, the General purpose Timer will start to count down from this current count value. If the user wishes to stop the counter and start from the original preload value or from a new preload value, this value will need to be rewritten into the Timer Preload register prior to the restarting of the General Purpose Timer register.

Note: The maximum clock period of the General Purpose Timer is 4295 seconds (1 hour, 11min & 35 Seconds).

2.7.5 Geographical Address Register

Address: A0 (H)
Length 16 bits

Read/Write The Geographical Address register shows the slot number of the VPX backplane where the *EXC-8000ccVPX* board is located. Bits 0–4 represent the slot number. Bit 5 is used for odd parity.

Bit	Description
06-15	Reserved – set to 0
05	Parity bit used for odd parity of the Geographical Address. This value of this bit is from pin GAPn in connector P0. See **3.4.1.1 Power Connector [P0] Pin Assignments** on page 3-5.
00-04	Geographical Address. The slot number of the VPX backplane where the *EXC-8000ccVPX* board is located. Slot 1 is the leftmost slot on the backplane. The values of these bits are from pins GA0 through GA4 in connector P0. See **3.4.1.1 Power Connector [P0] Pin Assignments** on page 3-5.

Table 2-15 Geographical Address Register

2.8 Module Memory Space Map

The module memory space map resides in the first memory block. Each module is allocated a space of 128 KB which is mapped as shown in **Figure 2-5 Module Memory Space Map.** (See **Chapter 4 Ordering Information** for information on the available modules for this carrier board.)

Reserved	3FFF FFFF H	A0000 H
Module #4	9FFFF H	80000 H
Module #3	7FFFF H	60000 H
Module #2	5FFFF H	40000 H
Module #1	3FFFF H	20000 H
Module #0	1FFFF H	00000 H

Figure 2-5 Module Memory Space Map

3 Mechanical and Electrical Specifications

Chapter 3 describes the mechanical and electrical specifications of the *EXC-8000ccVPX* carrier board. The following topics are covered:

3.1 Board Layout

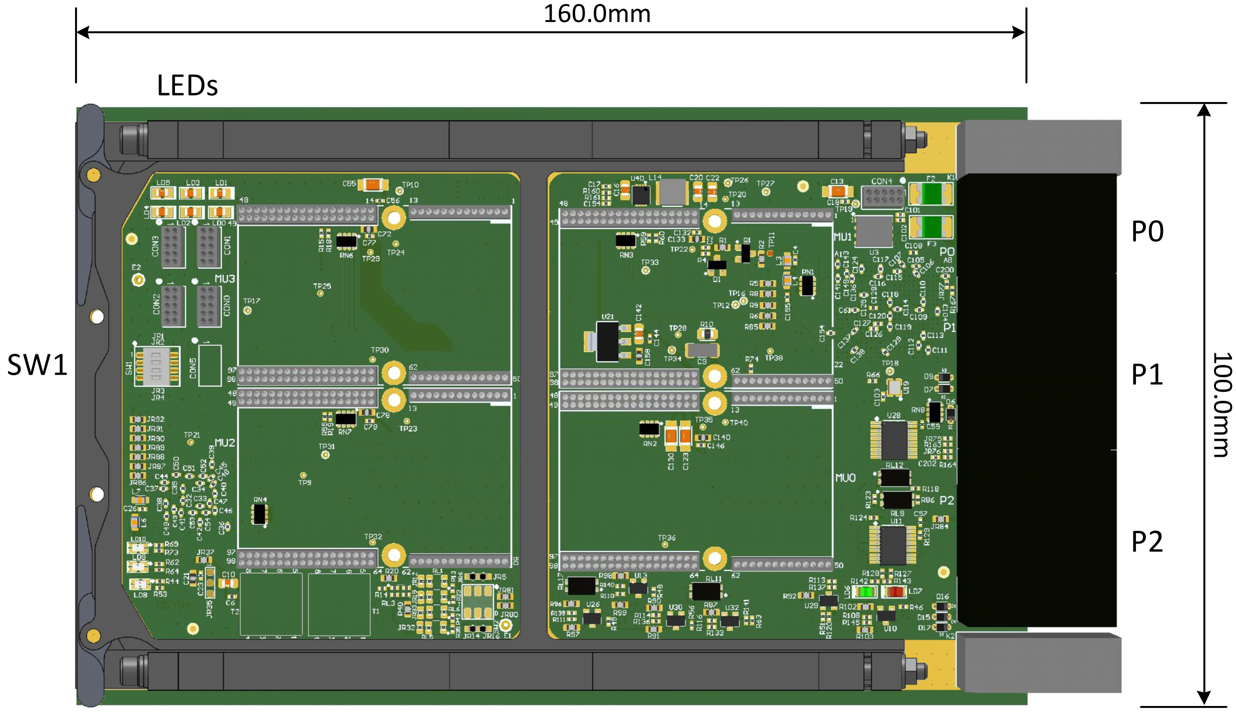

Figure 3-1 Board Layout

3.2 LED Indicators

The board contain five LEDs.

LED	Name	Indication
LD0	RDY0	Module 0 Ready
LD1	RDY1	Module 1 Ready
LD2	RDY2	Module 2 Ready
LD3	RDY3	Module 3 Ready
LD4	RDY4	Module 4 Ready

Table 3-1 Led Indicators

3.3 DIP Switches

The board contains one DIP switch (SW1).

3.3.1 Select ID DIP Switch [SW1]

This four contact DIP switch provides the board's 'Selected ID.' It represents a four bit number of which position #1 is the most significant bit. When a specific bit of the switch is:

- **Off** – a value of "1" will be set for that bit
- **On** – a value of "0" will be set for that bit

Multiple Board Applications

To provide a unique Selected ID, to identify a board by the application software in a multiple board application, the DIP switch should be set differently for each board in the same computer. For example:

	For Board ID#1	For Board ID#3
Bit 1	On	On
Bit 2	On	On
Bit 3	On	Off
Bit 4	Off	Off

Table 3-2 DIP Switch Settings for Unique Selected ID

For multiple board applications, each board's device number may be set by using the Excalibur configuration utility program provided with the drivers, and by setting the Unique ID to match that set on the DIP switch shown in Figure 3-2.

Select ID	Bit 1	Bit 2	Bit 3	Bit 4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1

Table 3-3 Selected ID Bits

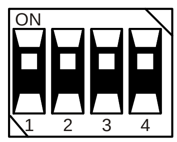

Figure 3-2 DIP Switch SW1 with All Switches Set to ON (Selected ID#0)

3.4 Connectors

The *EXC-8000ccVPX* contains the following connectors:

1. A 56-pin VPX power connector [P0]. The connector pinouts and signals are described in Table 3-4 on page 3-5.

P/N: Tyco® 1410189-3	Left End Half Module VPX Plug-in Connector

   The mating connector is:

P/N: Tyco® 1410186-1	Left End Half Module VPX Back Plane (Plug-in Mating) Connector

2. A 112-pin VPX differential connector [P1] for PCI Express signals. The connector pinouts and signals are described in Table 3-6 on page 3-7.

P/N: Tyco® 1410187-3	Center Module VPX Plug-in Differential Connector

   The mating connector is:

P/N: Tyco® 1410140-1	Center Module VPX Back Plane (Plug-in Mating) Connector

3. A 112-pin VPX differential connector [P2] for passing signals for all module I/O signals and the remaining external signals. The connector pinouts and signals are described in Table 3-8 on page 3-9.

P/N: Tyco® 1410187-3	Center Module VPX Plug-in Differential Connector

   The mating connector is:

P/N: Tyco® 1410140-1	Center Module VPX Back Plane (Plug-in Mating) Connector

3.4.1 Power Connector [P0]

A 56-pin (8-wafer PCB, 7-row) male MULTIGIG RT VPX plug-in left end half module VPX connector [P0] (P/N: Tyco® 1410189-3) provides all power required by the *EXC-8000ccVPX* board. It mates with P/N: Tyco® 1410186-1.

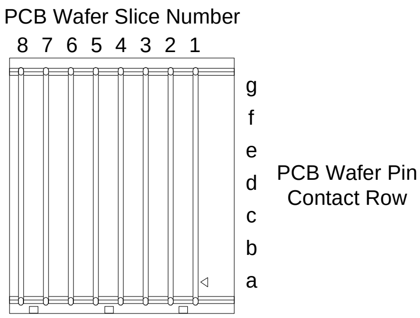

Figure 3-3 Power Connector [P0]

3.4.1.1 Power Connector [P0] Pin Assignments

Table 3-4 lists the signal names for each pin in Connector P0, and Table 3-5 describes the signals.

PCB Wafer Slice Number	PCB Wafer Pin Contact Row							
	Wafer Type	**Row G**	**Row F**	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**
1	**Power**	+12V	+12V	+12V	N/C	+3.3(Option)	+3.3(Option)	+3.3(Option)
2	**Power**	+12V	+12V	+12V	N/C	+3.3(Option)	+3.3(Option)	+3.3(Option)
3	**Power**	+5V(Option)	+5V(Option)	+5V(Option)	N/C	+5V(Option)	+5V(Option)	+5V(Option)
4	**Single-ended**	Reserved	Reserved	GND	N/C	GND	SYSRESETn	N/C
5	**Single-ended**	GAPn	GA4n	GND	3.3V_AUX	GND	Reserved	Reserved
6	**Single-ended**	GA3n	GA2n	GND	N/C	GND	GA1n	GA0n
7	**Differential**	N/C	GND	N/C	N/C	GND	N/C	N/C
8	**Differential**	GND	PCIe_REF_CLK-	PCIe_REF_CLK+	GND	N/C	N/C	GND

Table 3-4 Power Connector [P0] Pin Assignments

Note: The suffix 'n' represents an active low signal.

Signal Name	Description
+12V	+12V Power Supply (in)
+3.3V	+3.3 Power Supply (in) Option for legacy cards
+3.3V_AUX	+3.3 Power Supply (in)
+5V	+5V Power Supply (in), Option for legacy cards
GA0n through GA4	Geographical Addressing signals (in), active low functionality. The Geographical Address specifies which slot in the VPX back plane that the *EXC-8000ccVPX* is plugged into. On the VPX backplane these signals are grounded or left floating. All these signals are pulled up internally to 25K. The *EXC-8000ccVPX* board inverts the signals so that a grounded signal is saved in the register as a 1, and a floating signal is saved as a 0. GA0n corresponds to the least significant bit. In accordance with the VITA Specification 46.11, the value of the left most slot of the VPX backplane has a value of 1, the slot to its right has a value of 2, etc. See **2.7.5 Geographical Address Register** on page 2-18.
GAPn	Graphical Address Parity signal (in), active low functionality. This signal represents the odd parity of the sum of the grounded Geographical Address pins. If the sum of the grounded Geographical Address pins is an even number, this pin is grounded. The *EXC-8000ccVPX* board inverts this signal so that a grounded signal is saved in the register as a 1, and a floating signal is saved as a 0.
PCIe_REF_CLK+\-	PCI Express 100 MHz Differential Reference clock (in)
SYSRESETn	Global Reset Signal (in), active low
GND	Ground
Reserved	Reserved

Table 3-5 Power Connector [P0] Signal Descriptions

3.4.2 PCI Express and External Signals Connector [P1]

A 112-pin (16-wafer PCB, 7-row) male MULTIGIG RT VPX plug-in center module differential connector [P1] (P/N: Tyco® 1410187-3) provides all the required PCI Express and some external I/O signals. It mates with P/N: Tyco® 1410140-1.

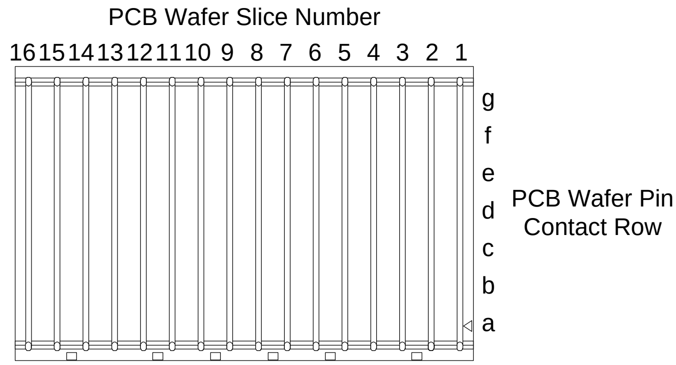

Figure 3-4 PCI Express and External Signals Connector [P1]

3.4.2.1 PCI Express and External Signals Connector [P1] Pin Assignments

Table 3-6 lists the signal names for each pin in Connector P1, and Table 3-7 describes the signals.

	PCB Wafer Pin Contact Row						
PCB Wafer Slice Number	**Row G**	**Row F**	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**
1	Reserved	GND	PCIe_Tx0_n	PCIe_Tx0_p	GND	PCIe_Rx0_n	PCIe_Rx0_p
2	GND	N/C	N/C	GND	N/C	N/C	GND
3	N/C	GND	N/C	N/C	GND	N/C	N/C
4	GND	N/C	N/C	GND	N/C	N/C	GND
5	N/C	GND	N/C	N/C	GND	N/C	N/C
6	GND	N/C	N/C	GND	N/C	N/C	GND
7	N/C	GND	N/C	N/C	GND	N/C	N/C
8	GND	N/C	N/C	GND	N/C	N/C	GND
9	EXTTCLKI	GND	N/C	N/C	GND	N/C	N/C
10	GND	N/C	N/C	GND	N/C	N/C	GND
11	EXTTRSTn	GND	N/C	N/C	GND	N/C	N/C
12	GND	N/C	N/C	GND	N/C	N/C	GND
13	Reserved	GND	N/C	N/C	GND	N/C	N/C
14	GND	N/C	N/C	GND	N/C	N/C	GND
15	Reserved	GND	N/C	N/C	GND	N/C	N/C
16	GND	N/C	N/C	GND	N/C	N/C	GND

Table 3-6 PCI Express and External Signals Connector [P1] Pin Assignments

Note: The suffix ‘n’ represents an active low signal.

Signal Name	Description
PCIe_Tx0_n	PCI Express x1 lane transmit output differential negative signal (output)
PCIe_Tx0_p	PCI Express x1 lane transmit output differential positive signal (output)
PCIe_Rx0_n	PCI Express x1 lane receive input differential pair negative signal (input)
PCIe_Rx0_p	PCI Express x1 lane receive input differential pair positive signal (input)
EXTTCLKI	**External Time Tag Clock Input.** This signal is received from an external source, and supplies a global clock for the Time Tags of all the modules. Use this signal to synchronize the Time Tags that are implemented on the modules[1] to other boards or systems.[2] See **2.5.7 Time Tag Clock Select Register** on page 2-13. This signal is a standard TTL input (Vih_min = 2.0V) with a nominal 1 MHz clock of 50% duty cycle (+/-10%) in reference to the ground pin. Our internal Time Tag clock source has a 50 ppm stability.
EXTTRSTn	**External Time Tag Reset TTL Input.** Use this low active pulsed signal (minimum 100 nsec.wide) to simultaneously reset the Time Tags of all the modules from an external source. Use the signal to synchronize these Time Tags to other boards or systems.[2]
GND	Ground
N/C	Not connected
RESERVED	Reserved

Table 3-7 PCI Express and External Signals Connector [P1] Signal Descriptions

1. See the manual for each module for a description of how the Time Tag clock is implemented, if used, for that module.
2. See **3.4.3.2 Synchronizing with an External Source** on page 3-15.

3.4.3 Modules I/O Signals Connector [P2]

A 112-pin (16-wafer PCB, 7-row) male MULTIGIG RT VPX plug-in center module differential connector [P2] (P/N: Tyco® 1410187-3) provides all the module's I/O signals and the remaining external signals. It mates with P/N: Tyco® 1410140-1.

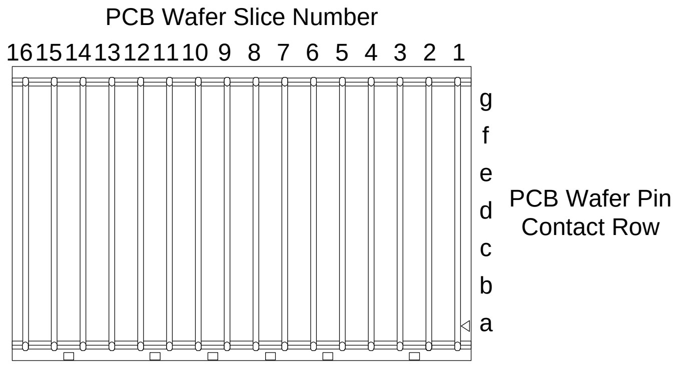

Figure 3-5 Modules I/O Signals Connector [P2]

3.4.3.1 Modules I/O Signals Connector [P2] Pin Assignments

Table 3-8 lists the signal names for each pin in Connector P2. The signal descriptions vary depending on the module installed in each module location. Tables 3-9 through 3-13 describe the signals for each module type.

	PCB Wafer Pin Contact Row						
PCB Wafer Slice Number	**Row G**	**Row F**	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**
1	RESERVED	GND	M1CH1L	M1CH1H	GND	M1CH0L	M1CH0H
2	GND	M1CH3L	M1CH3H	GND	M1CH2L	M1CH2H	GND
3	RESERVED	GND	M1CH5L	M1CH5H	GND	M1CH4L	M1CH4H
4	GND	M0CH1L	M0CH1H	GND	M0CH0L	M0CH0H	GND
5	N/C	GND	M0CH3L	M0CH3H	GND	M0CH2L	M0CH2H
6	GND	M0CH5L	M0CH5H	GND	M0CH4L	M0CH4H	GND
7	N/C	GND	SHIELD	SHIELD	GND	SHIELD	SHIELD
8	GND	M3CH1L	M3CH1H	GND	M3CH0L	M3CH0H	GND
9	N/C	GND	M3CH3L	M3CH3H	GND	M3CH2L	M3CH2H
10	GND	M3CH5L	M3CH5H	GND	M3CH4L	M3CH4H	GND
11	N/C	GND	M2CH1L	M2CH1H	GND	M2CH0L	M2CH0H
12	GND	M2CH3L	M2CH3H	GND	M2CH2L	M2CH2H	GND
13	IRIGB	GND	M2CH5L	M2CH5H	GND	M2CH4L	M2CH4H
14	GND	M4DIO0	M4DIO1	GND	M4DIO5	M4DIO6	GND
15	GNDD04	GND	M4DIO2	SHIELD	GND	M4DIO7	GNDD59
16	GND	M4DIO3	M4DIO4	GND	M4DIO8	M4DIO9	GND

Table 3-8 Modules I/O Signals Connector [P2] Pin Assignments

Table 3-9 describes the Connector P2 signals for the *M8K429RT5*, *M8K717*, *M8K825CAN*, *M8KSerial*, *M8KMMSI* and *M8KDiscrete* modules. In this table, the **M*x*** in the signal name stands for M0, M1, M2 or M3.

Signal Name	Description							
	M8K429RT5	**M8K717**	**M8K825CAN**	**M8KSerial RS-232**	**M8KSerial RS-422**	**M8KSerial RS-485**	**M8KMMSI**	**M8KDiscrete**
M*x*CH0L	Channel 0 Low	N/C	Channel 0 Low	N/C	Channel 0 Transmit High	Channel 0 High	Channel 0 Low	I/O Channel 0
M*x*CH0H	Channel 0 High	N/C	Channel 0 High	Channel 0 Transmit	Channel 0 Transmit Low	Channel 0 Low	Channel 0 High	I/O Channel 1
M*x*CH1L	Channel 1 Low	N/C	Channel 1 Low	Channel 0 Receive	Channel 0 Receive High	N/C	Channel 1 Low	I/O Channel 2
M*x*CH1H	Channel 1 High	N/C	Channel 1 High	N/C	Channel 0 Receive Low	N/C	Channel 1 High	I/O Channel 3
M*x*CH2L	Channel 2 Low	N/C	Channel 2 Low	Ground	Ground	Ground	Channel 2 Low	I/O Channel 4
M*x*CH2H	Channel 2 High	N/C	Channel 2 High	Shield	Shield	Shield	Channel 2 High	Provides ground reference for Discretes 0–4
M*x*CH3L	Channel 3 Low	N/C	Channel 3 Low	N/C	Channel 1 Transmit High	Channel 1 High	Channel 3 Low	I/O Channel 5
M*x*CH3H	Channel 3 High	N/C	Channel 3 High	Channel 1 Transmit	Channel 1 Transmit Low	Channel 1 Low	Channel 3 High	I/O Channel 6
M*x*CH4L	Channel 4 Low	Transmit Channel Low	Channel 4 Low	Channel 1 Receive	Channel 1 Receive High	N/C	Channel 4 Low	I/O Channel 7
M*x*CH4H	Channel 4 High	Transmit Channel High	Channel 4 High	N/C	Channel 1 Receive Low	N/C	Channel 4 High	I/O Channel 8
M*x*CH5L	Reserved	Receive Channel Low	Reserved	Ground	Ground	Ground	Channel 5 Low	I/O Channel 9
M*x*CH5H	Reserved	Receive Channel High	Reserved	Shield	Shield	Shield	Channel 5 High	Provides ground reference for Discretes 5–9
GND	Provides ground reference for input and output channels							
SHIELD	Provides the input and output channels with shield connections							
IRIGB	**IRIG B120 Input.** The signal should have the following specifications: B = 100 pulses per second (PPS), 10 msec count 1 = Sine wave carrier, amplitude modulated 2 = 1 kHz carrier wave (1 msec resolution) 0 = Binary Coded Decimal (BCD), Control Functions (CF) depending on the user application, Straight Binary Second (SBS) of day (0 – 86400). The IRIG B signal should have a 3:1 modulation ratio at 3V typical.							
N/C	Not connected							

Table 3-9 Connector P2 Signal Descriptions for *M8K429RT5*, *M8K717*, *M8K825CAN*, *M8KSerial*, *M8KMMSI* and *M8KDiscrete* Modules

Table 3-10 describes the Connector P2 signals for the *M8K1553Px, M8K1760Px* and *M8K708* modules.

Signal Name	**Description**		
	M8K1553Px/ M8K1760Px	**M8K1553PxS/ M8K1760PxS**	**M8K708**
MxCH0L	BUS_AL	BUS_AL	CH0_L
MxCH0H	BUS_AH	BUS_AH	CH0_H
MxCH1L		RTA0	
MxCH1H		RTA1	
MxCH2L		RTA2	
MxCH2H		RTA3	
MxCH3L		RTA4	
MxCH3H		RTAPRTY	
MxCH4L	BUS_BL	BUS_BL	CH1_L
MxCH4H	BUS_BH	BUS_BH	CH1_H
MxCH5L		RTALOCK	
MxCH5H		GND	
GND	Provides ground reference for input and output channels		
SHIELD	Provides the input and output channels with shield connections		
IRIGB	**IRIG B120 Input.** The signal should have the following specifications: B = 100 pulses per second (PPS), 10 msec count 1 = Sine wave carrier, amplitude modulated 2 = 1 kHz carrier wave (1 msec resolution) 0 = Binary Coded Decimal (BCD), Control Functions (CF) depending on the user application, Straight Binary Second (SBS) of day (0 – 86400). The IRIG B signal should have a 3:1 modulation ratio at 3V typical.		
N/C	Not connected		

Table 3-10 Connector P2 Signal Descriptions for *M8K1553Px, M8K1760Px* and *M8K708* Modules

Table 3-11 describes the Connector P2 signals for the *M8KH009* module.

Signal Name	Description
MxCH0L	Data Bus A Low
MxCH0H	Data Bus A High
MxCH1L	Clock Bus A Low
MxCH1H	Clock Bus A High
MxCH2L	Shield
MxCH2H	Ground
MxCH3L	Data Bus B Low
MxCH3H	Data Bus B High
MxCH4L	Clock Bus B Low
MxCH4H	Clock Bus B High
MxCH5L	Shield
MxCH5H	Reserved
GND	Provides ground reference for input and output channels
SHIELD	Provides the input and output channels with shield connections
IRIGB	**IRIG B120 Input.** The signal should have the following specifications: B = 100 pulses per second (PPS), 10 msec count 1 = Sine wave carrier, amplitude modulated 2 = 1 kHz carrier wave (1 msec resolution) 0 = Binary Coded Decimal (BCD), Control Functions (CF) depending on the user application, Straight Binary Second (SBS) of day (0 – 86400). The IRIG B signal should have a 3:1 modulation ratio at 3V typical.
N/C	Not connected

Table 3-11 J1 Connector Pinouts for Double-Sized *M8KH009* Module

Table 3-12 describes the Connector P2 signals for the *M8KADDA* module.

Signal Name	Description					
	M8KADDA-P1 (DAC)		M8KADDA-P2 (ADC)		M8KADDA-P3 (DAC & ADC)	
	Single Ended	Differential	Single Ended	Differential	Single Ended	Differential
MxCH0L	Channel 0 Output	Channel 0/1 Output High	Channel 0 Input	Channel 0/1 Input High	Channel 0 Output	Channel 0/1 Output High
MxCH0H	Channel 1 Output	Channel 0/1 Output Low	Ground Reference Input	Channel 0/1 Input Low	Channel 1 Output	Channel 0/1 Output Low
MxCH1L	Channel 2 Output	Channel 2/3 Output High	Channel 2 Input	Channel 2/3 Input High	Channel 2 Output	Channel 2/3 Output High
MxCH1H	Channel 3 Output	Channel 2/3 Output Low	Ground Reference Input	Channel 2/3 Input Low	Channel 3 Output	Channel 2/3 Output Low
MxCH2L	Channel 4 Output	Channel 4/5 Output High	Channel 4 Input	Channel 4/5 Input High	Channel 4 Input	Channel 4/5 Input High
MxCH2H	Channel 5 Output	Channel 4/5 Output Low	Ground Reference Input	Channel 4/5 Input Low	Ground Reference Input	Channel 4/5 Input Low
MxCH3L	Channel 6 Output	Channel 6/7 Output High	Channel 6 Input	Channel 6/7 Input High	Channel 6 Input	Channel 6/7 Input High
MxCH3H	Channel 7 Output	Channel 6/7 Output Low	Ground Reference Input	Channel 6/7 Input Low	Ground Reference Input	Channel 6/7 Input Low
MxCH4L	Channel 8 Output	Channel 8/9 Output High	Channel 8 Input	Channel 8/9 Input High	Channel 8 Input	Channel 8/9 Input High
MxCH4H	Channel 9 Output	Channel 8/9 Output Low	Ground Reference Input	Channel 8/9 Input Low	Ground Reference Input	Channel 8/9 Input Low
MxCH5L	Ground	Ground	Ground	Ground	Ground	Ground
MxCH5H	Ground	Ground	Ground	Ground	Ground	Ground
GND	Provides ground reference for input and output channels					
SHIELD	Provides the input and output channels with shield connections					
IRIGB	**IRIG B120 Input.** The signal should have the following specifications: B = 100 pulses per second (PPS), 10 msec count 1 = Sine wave carrier, amplitude modulated 2 = 1 kHz carrier wave (1 msec resolution) 0 = Binary Coded Decimal (BCD), Control Functions (CF) depending on the user application, Straight Binary Second (SBS) of day (0 – 86400). The IRIG B signal should have a 3:1 modulation ratio at 3V typical.					
N/C	Not connected					

Table 3-12 J1 Connector Pinouts for the *M8KADDA* Module

Table 3-13 describes the Connector P2 signals for Module 4, the onboard *M8KDiscrete* module.

Signal Name	Description
M4DIO0	I/O Channel 0
M4DIO1	I/O Channel 1
M4DIO2	I/O Channel 2
M4DIO3	I/O Channel 3
M4DIO4	I/O Channel 4
M4DIO5	I/O Channel 5
M4DIO6	I/O Channel 6
M4DIO7	I/O Channel 7
M4DIO8	I/O Channel 8
M4DIO9	I/O Channel 9
GNDD04	Provides ground reference for Discretes 0–4
GNDD59	Provides ground reference for Discretes 5–9
GND	Provides ground reference for input and output channels
SHIELD	Provides the input and output channels with shield connections
IRIGB	**IRIG B120 Input.** The signal should have the following specifications: B = 100 pulses per second (PPS), 10 msec count 1 = Sine wave carrier, amplitude modulated 2 = 1 kHz carrier wave (1 msec resolution) 0 = Binary Coded Decimal (BCD), Control Functions (CF) depending on the user application, Straight Binary Second (SBS) of day (0 – 86400). The IRIG B signal should have a 3:1 modulation ratio at 3V typical.
N/C	Not connected

Table 3-13 Connector P2 Signal Descriptions for *M8KDiscrete* Module

3.4.3.2 Synchronizing with an External Source

To synchronize a single board to an external system, the external clock source and the external reset must be connected to the EXTTCLKI and the EXTTRSTn signals respectively.

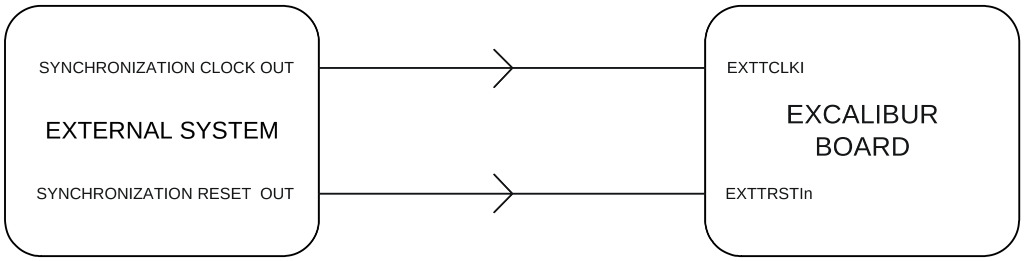

Figure 3-6 Synchronization of a Single Board to an External System

3.5 Power Requirements

The standby power requirements, without any modules installed, are:

150mA @ +12V

The final power requirements will depend on how many and which modules are installed. To calculate the exact board power requirements, see the specific module's user's manual.

Note: There is an option for legacy power (+5V/+3V supply). For more information, contact Excalibur Sales. See **1.3 Technical Support** on page 1-6.

4 Ordering Information

Chapter 4 explains which options to indicate when ordering.

Basic Part #	Option	Description
EXC-8000ccVPX/*xx*		Multiprotocol carrier board for VPX compatible systems. Replace '***xx***' with the module codes of the modules you want. See Table 4-2. For part number examples, see **4.1 Part Number Examples** on page 4-3. When ordering the board without modules, leave the '***xx***' in the part number. When ordering a module separate from a carrier board, use the module part # in Table 4-2. See the user's manual of the module for complete ordering information.
	-E	Extended temperature/ruggedized version. All the modules come with a ruggedized, extended temperature option (-40° to + 85°C).
	-001	With conformal coating

Table 4-1 Ordering Information

Table 4-2 lists the part numbers for the available modules.

Protocol Type	Module Part #	Module Code	Description
ARINC 429	**M8K429RT5**	**A0**	ARINC 429 module with 5 channels, software selectable as transmit or receive.
ARINC 708/453	**M8K708**	**C0**	ARINC 708/453 with 2 channels, software selectable as transmit or receive.
ARINC 717	**M8K717-Nx**	**N*x***	ARINC 717 module with 2 channels, one transmit and one receive. Replace '**N*x***' with one of the following: **N1** = HBP transmit channel **N2** = BPRZ transmit channel
ARINC 825	**M8K825CAN-S5**	**S5**	ARINC 825 module with 5 channels.
MIL-STD-1553	**M8K1553Px**	**F0**	MIL-STD-1553 multi-function module, selectable as Transformer or Direct coupled via a DIP switch.
MIL-STD-1553 Monitor Only	**M8K1553PxM**	**G0**	MIL-STD-1553 multi-function module for monitoring only, selectable as Transformer or Direct coupled via a DIP switch.
MIL-STD-1553 Single Function	**M8K1553PxS**	**T*x***	MIL-STD-1553 single function module. Replace '**Tx**' with one of the following: **T1** = PxS Transformer coupled mode **T2** = PxS Direct coupled mode
MIL-STD-1553 Single Function Monitor Only	**M8K1553PxSM**	**V*x***	MIL-STD-1553 module for monitoring only. Replace '**Vx**' with one of the following: **V1** = PxS Transformer coupled mode **V2** = PxS Direct coupled mode

Table 4-2 Module Codes

Protocol Type	Module Part #	Module Code	Description
MIL-STD-1760	**M8K1760Px**	**L0**	MIL-STD-1760 multi-function module, selectable as Transformer or Direct coupled via a DIP switch.
MIL-STD-1760 Monitor Only	**M8K1760PxM**	**M0**	MIL-STD-1760 multi-function module for monitoring only, selectable as Transformer or Direct coupled via a DIP switch.
MIL-STD-1760 Single Function	**M8K1760PxS**	**H*x***	MIL-STD-1760 single function module. Replace '**Hx**' with one of the following: **H1** = PxS Transformer coupled mode **H2** = PxS Direct coupled mode
MIL-STD-1760 Single Function Monitor Only	**M8K1760PxSM**	**K*x***	MIL-STD-1760 module for monitoring only. Replace '**Kx**' with one of the following: **K1** = PxS Transformer coupled mode **K2** = PxS Direct coupled mode
MMSI	**M8KMMSI-R5**	**R5**	MMSI module with 5 EBR hub ports and 1 cBM port.
H009	**M8KH009**	**D0**	H009 interface module. This is a double-sized module and occupies two modules locations. It can be installed in module locations 0–1 or 2–3.
Discrete	**M8KDiscrete**	**I0**	Discrete module with 10 bi-directional Discretes with TTL (0 to 5 volts) or avionics (0 to 32 volts) voltage levels.
Serial	**M8KSerial-J*x***	**J*x***	Serial module with 2 channels, software selectable for RS-232 up to 3 Mbps and RS-422 and RS-485 up to 4 Mbps. Replace '**J*x***' with one of the following: **J1** = Channel 0 is RS-232; Channel 1 is RS-232 **J2** = Channel 0 is RS-232; Channel 1 is RS-485 **J3** = Channel 0 is RS-232; Channel 1 is RS-422 **J4** = Channel 0 is RS-485; Channel 1 is RS-485 **J5** = Channel 0 is RS-485; Channel 1 is RS-422 **J6** = Channel 0 is RS-422; Channel 1 is RS-422
ADDA	**M8KADDA**	**P*x***	A/D and D/A module. Replace '**P*x***' with one of the following: **P1** = DAC outputs only, 10 single ended or 5 differential **P2** = ADC inputs only, 5 single ended or 5 differential **P3** = Combined DAC and ADC 4 single ended or 2 differential DAC outputs and 3 single ended or 3 differential ADC inputs

Table 4-2 Module Codes (Continued)

4.1 Part Number Examples

When ordering a board with a number of different protocol modules, the module codes must be in the following form:

EXC-8000ccVPX/A0B1C0D0

The first module code (A0) in the part number is Module 0, the second (B1) is Module 1, and so on.

If one or more empty module locations are required in between other modules, insert an asterisk (*). Also, an asterisk (*) is required before the module code of a double-sized module for alignment purposes.

Example: EXC-8000ccVPX/J2J3

This is an *EXC-8000ccVPX* board with:
An *M8KSerial* module (J2) with channel 0 as RS-232 and channel 1 as RS-485 at module location 0.
An *M8KSerial* module (J3) with channel 0 as RS-232 and channel 1 as RS-422 at module location 1.
Module locations 2 and 3 are empty.
The onboard *Discrete* module is at module location 4.

Example: EXC-8000ccVPX/A0*F0

This is an *EXC-8000ccVPX* board with:
An *M8K429RT5* module (A0) at module location 0.
Module location 1 is empty (*).
An *M8K1553Px* module (F0) at module location 2.
Module location 3 is empty.
The onboard *Discrete* module is at module location 4.

Example: EXC-8000ccVPX/J6T1*D0

This is a *EXC-8000ccVPX* with:
An *M8KSerial* module (J6) with two RS-422 channel at module location 0.
An *M8K1553PxS* single function Transformer coupled module (T1) at module location 1.
An *M8KH009* interface double-sized module (*D0) at module locations 2 and 3. An asterisk (*) is required before the module code of a double-sized module for alignment purposes.
The onboard *Discrete* module is at module location 4.

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